Nos. 2022-1293, 2022-1294, 2022-1295, 2022-1296

United States Court of Appeals for the Federal Circuit

IN RE: CELLECT, LLC,
Appellant

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board, in Nos. 90/014,453, 90/014,454, 90/014,455, 90/014,457

CELLECT, LLC'S PRINCIPAL BRIEF

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REPRESENTATIVE CLAIMS

U.S. Patent No. 6,982,742

42. In a PDA having capability to transmit and receive data in a communications network, the improvement comprising:

a video system integral with said PDA for receiving and transmitting video images, and for viewing said images, said video system comprising:

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically coupled to said image sensor, said first circuit board including circuitry means for timing and control of said array of pixels and circuitry means for processing and converting said pre-video signal to a desired video format, a transceiver radio element communicating with said firs circuit board for transmitting said converted pre-video signal;

a transceiver radio module mounted in said PDA for wirelessly receiving said converted pre-video signal; and

a video view screen attached to said PDA for viewing said video images, said video view screen communicating with said transceiver radio module, and displaying video images processed by said first circuit board.

U.S. Patent No. 6,424,369

49. In a PDA having capability to transmit data between a personal computer connected to a communications network, the improvement comprising:

a video system integral with said PDA for receiving and transmitting video images, and for viewing said images, said video system comprising:

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically coupled to said image sensor, said first circuit board including circuitry means for timing and control of said array of CMOS pixels and circuitry means for processing and converting said pre-video signal to a desired video format; and

a video view screen attached to said PDA for viewing said video images, said video view screen communicating with said first circuit board.

U.S. Patent No. 6,452,626

1. In a wireless telephone for conducting wireless telephonic communications, the improvement comprising:

a video system integral with said telephone for receiving and transmitting video images, and for viewing said video images, said video system comprising;

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of CMOS pixels for timing and control of said array of CMOS pixels, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically coupled to said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;

a video monitor attached to said wireless phone for viewing said video images, said video monitor communicating with said first circuit board, and displaying video images processed by said first circuit board.

U.S. Patent No. 7,002,621

33. In a video telephone for receiving and transmitting telephone communications to include video signals transmitted by the user of the phone, and video signals received from the party to whom a call is made, the video telephone including a video monitor for viewing the video signals, the improvement comprising:

a camera module for taking video images, said camera module communicating with circuitry within said video enabling video signals to be transmitted from said camera module to said video telephone for viewing by said user or for further transmission to another party, said camera module including an image sensor housed therein and lying in a first plane, said image sensor including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal, and a transceiver radio element communicating with said image sensor for wirelessly transmitting said pre-video signal.

CERTIFICATE OF INTEREST

Counsel for Cellect, LLC certifies the following:

1. The full name of every entity represented by us is:

   Cellect, LLC.

2. The name of the real party in interest for the entity. Do not list the real party if it is the same as the entity:

   Not applicable.

3. All parent corporations and any other publicly held companies that own 10 percent or more of the stock of the party or amicus curia represented by me are listed below:

   Cellect, LLC is a wholly-owned subsidiary of Micro Imaging Solutions LLC.

4. The names of all law firms, and the partners or associates that have not entered an appearance in the appeal, and (a) appeared for the entity in the lower tribunal; or (b) are expected to appear for the entity in this court:

   Not applicable.

5. Other than the originating case number(s), the title and number of any case known to counsel to be pending in this or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal:

   - *In Re: Cellect, LLC*, No. 22-1292 (Fed. Cir.); and
   - *Cellect, LLC v. Samsung Electronics Co., Ltd., et al.*, No. 1:19-cv-00438 (D. Colo.).

6. All information required by Fed. R. App. P. 26.1(b) and (c) in criminal cases and bankruptcy cases.

   None.

Dated: May 16, 2022

By: */s/ Paul J. Andre*

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STATEMENT OF RELATED CASES

Pursuant to Federal Circuit Rule 47.5, Cellect, LLC states that:

No appeal in this case was previously before this Court or any other court.

The following case is pending before this Court regarding U.S. Patent No. 6,982,740:

- *In Re: Cellect, LLC*, No. 22-1292 (Fed. Cir.).

The following case is pending before the United States District Court for the District of Colorado regarding U.S. Patent Nos. 6,982,740, 6,982,742, 6,424,369, 6,452,626, and 7,002,621:

- *Cellect, LLC v. Samsung Electronics Co., Ltd., et al.*, No. 1:19-cv-00438 (D. Colo.).

JURISDICTION

On December 1, 2021, the U.S. Patent Trial and Appeal Board issued four Decisions on Appeal in Reexamination Control Nos. 90/014,453 (Appx1-25), 90/014,454 (Appx26-49), 90/014,455 (Appx50-74), and 90/014,457 (Appx75-97). Patent Owner, Cellect, LLC, timely filed a Notice of Appeal in each reexamination on December 21, 2021. Appx4136-4141, Appx6381-6386, Appx9260-9267, Appx12114-12119. This Court has jurisdiction over this appeal pursuant to 28 U.S.C. § 1295(a)(4)(A).

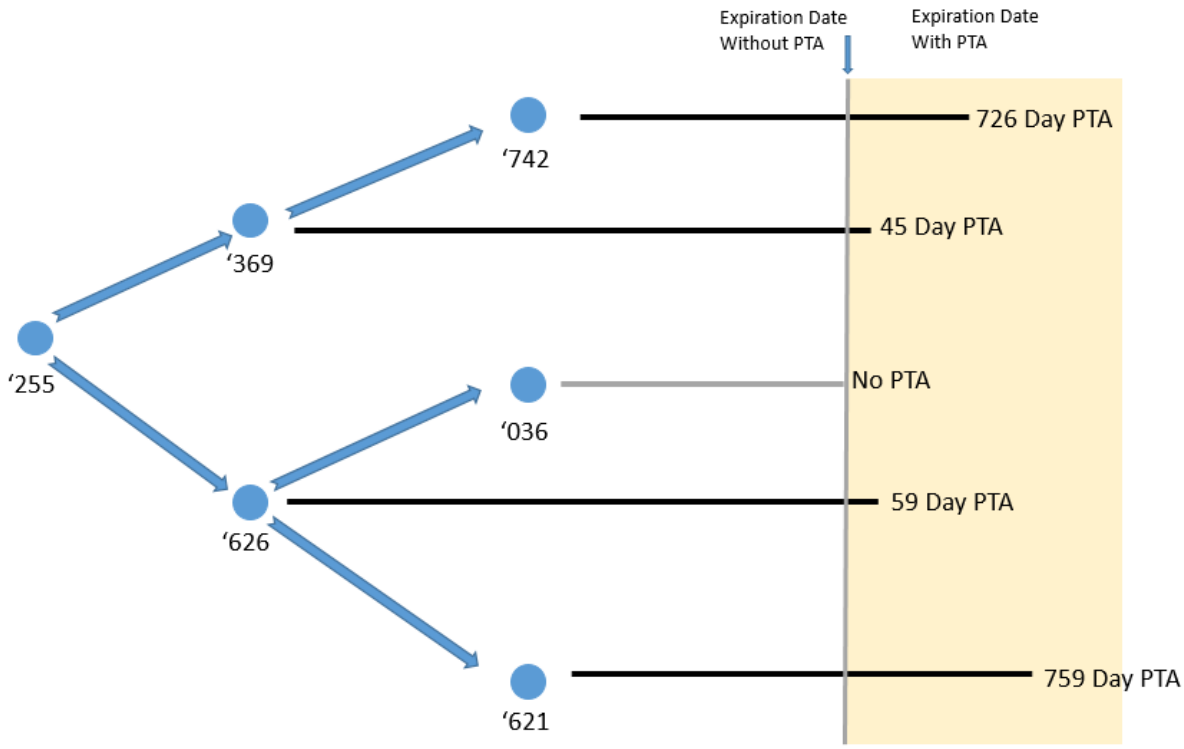
INTRODUCTION

The U.S. Patent Trial and Appeal Board ("the Board") created an artificial distinction between patent term extension (or "PTE") and patent term adjustment (or "PTA") for purposes of non-statutory obviousness-type double patenting (or "double patenting") that runs contrary to this Court's guidance and other District Courts' holdings. These types of statutorily authorized time extensions do not run afoul of the judicially created doctrine of double patenting because they do not permit "***improper*** timewise extension of the patent right." *In re Bradt*, 937 F.2d 589, 592 (Fed. Cir. 1991) (emphasis added). Indeed, the time extensions from PTA and PTE are ***properly*** granted by statute—35 U.S.C. §§ 154(b) and 156. Nonetheless, the Board determined that judicially created "non-statutory" double patenting trumps mandated "statutory" PTA for validity purposes for a family of patents under common ownership.

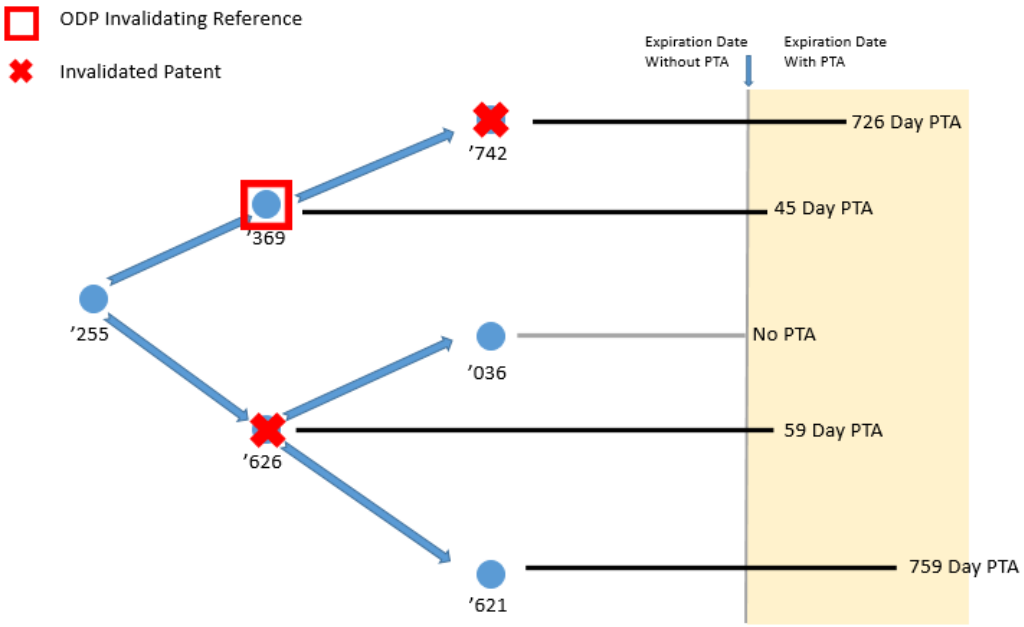
Doubling down on this flawed logic, the Board used a hodgepodge of related patents to find a substantial new question of patentability during reexamination and invalidated four related patents under the guise of double patenting (the "Challenged Patents").[1] The figures below show the patents' relationship and how the Board weaponized certain Cellect patents to invalidate every patent with a PTA.

[1] The Challenged Patents are U.S. Patent No. 6,982,742 ("the '742 Patent"), U.S. Patent No. 6,424,369 ("the '369 Patent"), U.S. Patent No. 6,452,626 ("the '626 Patent), and U.S. Patent No. 7,002,621 ("the '621 Patent").

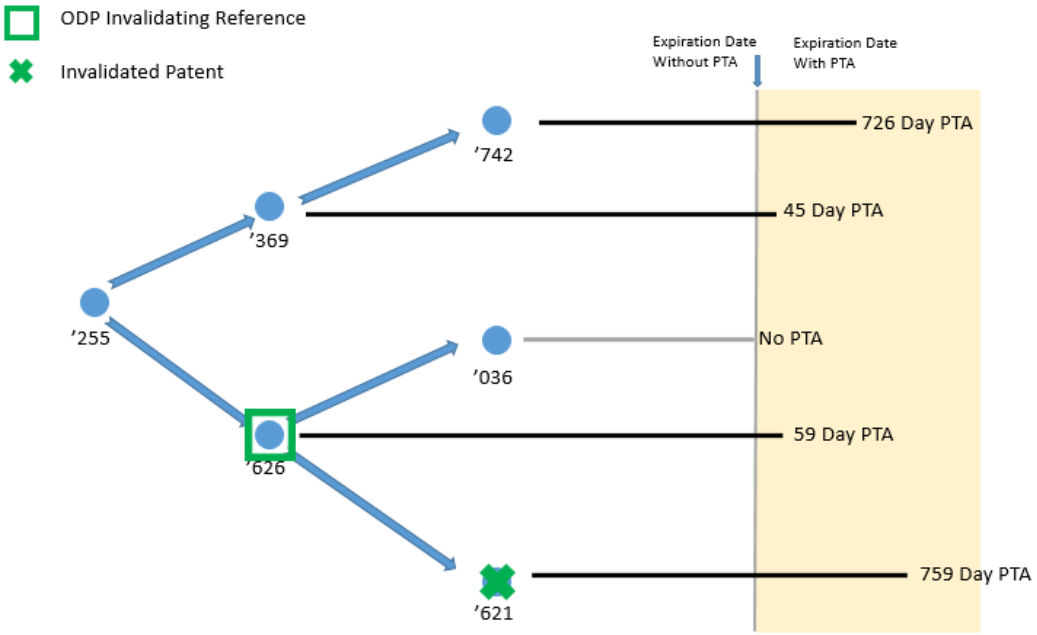
Below is the relationship amongst the Cellect patents and their original expiration date relative to the adjusted expiration dates.



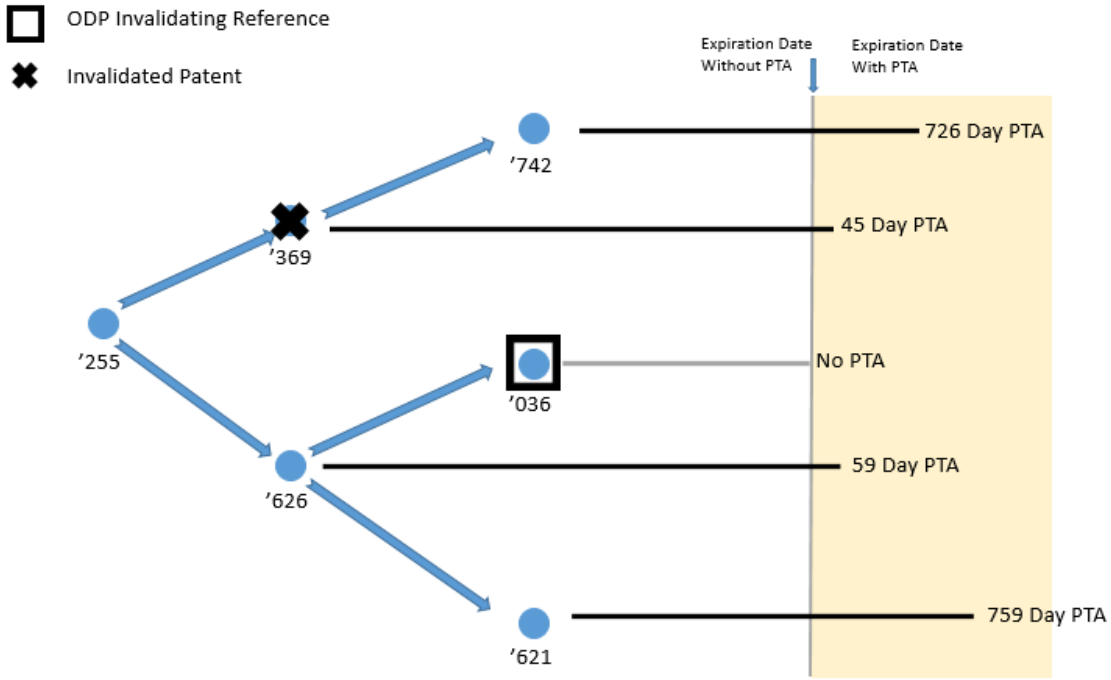
First, the Board used the '369 Patent against its own child, the '742 Patent, and against its sister, the '626 Patent, as shown below.



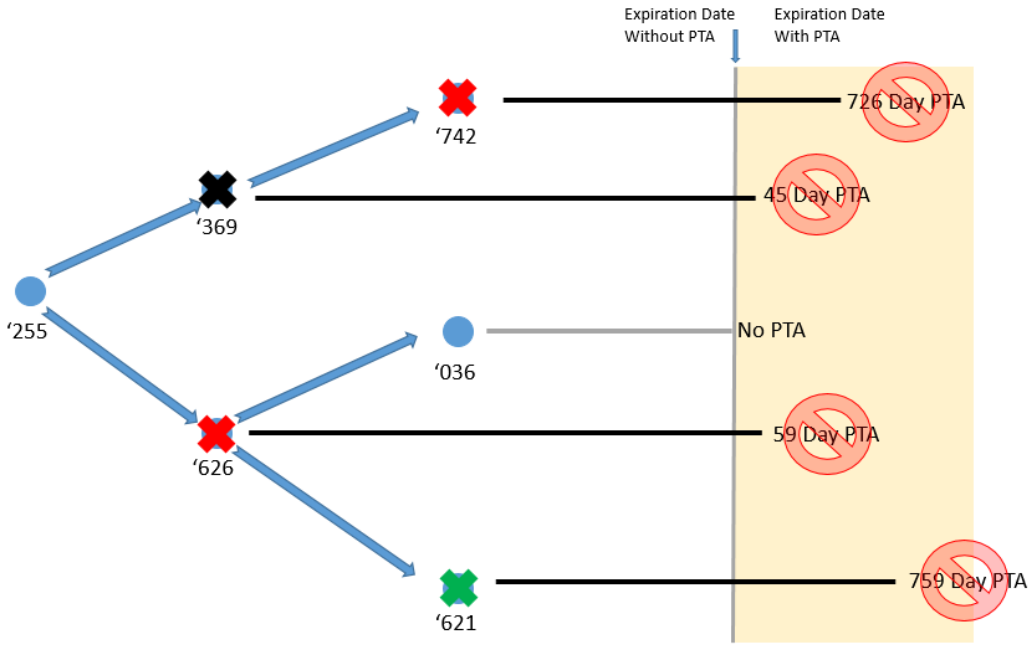
Next, the Board used the '626 Patent against its own child, the '621 Patent. (As shown above, however, the '626 Patent was itself invalidated by its brother, the '369 Patent.)



Finally, the Board used U.S. Patent No. 6,862,036 ("the '036 Patent") against its uncle, the '369 Patent.



By the time the Board finished turning one family member against another, it had invalidated every patent with a PTA based on double patenting, as pictured below.



The Board's whack-a-mole logic found every term-adjusted patent invalid under double patenting based solely on the patents' expiration dates. The Board used an equitable doctrine to achieve an inequitable result. To wit, Cellect had no opportunity to cure the ***alleged*** improper term adjustment because the cure (*i.e.*, a terminal disclaimer) was unavailable in the reexaminations because the Cellect patents had expired when the double patenting rejection was made, whereas Cellect could have filed a terminal disclaimer during the original prosecution if the issue had been raised. Under the Board's interpretation of PTA and how it relates to double patenting, every inventor would need to file preemptive terminal disclaimers during prosecution to avoid having related patents invalidate one another under double patenting, resulting in the abrogation of 35 U.S.C. § 154(b) altogether.

Moreover, the Board ignored the specific facts surrounding the prosecution of the Cellect patents that demonstrated that the PTAs were ***proper*** term extensions. The same Patent Examiner, Anand Rao, was responsible for examination of all of Cellect's Challenged Patents and the '036 Patent (collectively "the Patents at Issue"). He was aware of the claims, that the U.S. Patent and Trademark Office ("Patent Office") had granted PTAs, and determined that double patenting was not applicable. Thus, there cannot be any ***substantial new*** question of patentability. Nonetheless, the Board weaponized these adjustments to invalidate related patents,

even though "[a] difference in expiration dates between two patents that arises solely from a statutorily authorized time extension, such as a patent-term adjustment pursuant to 35 U.S.C. § 154(b) or a patent-term extension pursuant to 35 U.S.C. § 156, cannot be the basis for an application of [double patenting]." *Amgen, Inc. v. Sandoz Inc.*, No. 18-11026 (MAS) (DEA), 2021 WL 5366800, at *26-27 (D.N.J. Sept. 20, 2021), *appealed on other grounds*, No. 22-1147 (lead) (Fed. Cir. Nov. 12, 2021) (citing *Novartis AG v. Ezra Ventures, LLC*, 909 F.3d 1367, 1372-75 (Fed. Cir. 2018) (rejecting attempt to use "a judge-made doctrine" to "cut off a statutorily-authorized time extension")) (further citation omitted).

STATEMENT OF ISSUES

1. Whether patent term adjustments should be treated in the same way as patent term extensions for purposes of non-statutory obviousness-type double patenting.

2. Whether a patent can become a basis for double patenting against another related patent, when the only reason that the two related patents expire at different times was due to a statutorily granted patent term adjustment.

3. Whether the Board erred in finding that double patenting raised a substantial new question of patentability during reexamination when the evidence demonstrates that the Patent Office considered double patenting during prosecution and knew about the term adjustments during prosecution.

STATEMENT OF THE CASE

Two generations of the Adair family, Dr. Edwin L. Adair, a renowned urologist and prolific inventor, and his sons Jeffrey Adair and John Adair, founded Appellant Cellect, LLC ("Cellect") and its parent company, Micro Imaging Solutions LLC. Appx1745, Appx1751, ¶¶ 2, 21. Together, this innovative family pioneered and developed complementary metal-oxide semiconductor ("CMOS") imaging technology. *See generally* Appx1745-1751 (Declaration of Cellect's Chief Technology Officer), ¶¶ 2-21. They were awarded numerous patents, and the Cellect family of Patents at Issue disclose CMOS camera technology that has important applications in modern smartphones and tablets. Appx1750-1751, ¶¶ 16-21. Dr. Adair, his brother Randall Adair, and Mr. Jeffrey Adair are the inventors of the Challenged Patents at issue in this appeal. Appx132, Appx163, Appx189, Appx216.

Cellect appeals four Board Decisions affirming the invalidity of certain claims of the Challenged Patents in *ex parte* reexaminations based on double patenting due to the Patent Office granting a patent term adjustment. *See generally* Appx1-25, Appx26-49, Appx50-74, Appx75-97 (Decisions on Appeal for Reexamination Control Nos. 90/014,453, 90/014,454, 90/014,455, and 90/014,457, respectively) (collectively "Decisions"). The Challenged Patents and claims at issue in these Decisions are:

- Claims 22, 42, 58, and 66 of the ’742 Patent;
- Claims 1, 17, 19, 21, 22, 27, 49, 55, and 61 of the ’369 Patent;
- Claims 1, 5, 11, 33, 34, 58, and 64 of the ’626 Patent; and
- Claims 25, 26, 27, 28, 29, and 33 of the ’621 Patent.

A. Cellect’s Challenged Patents Are from the Same Patent Family and Claim Priority to the Same Application

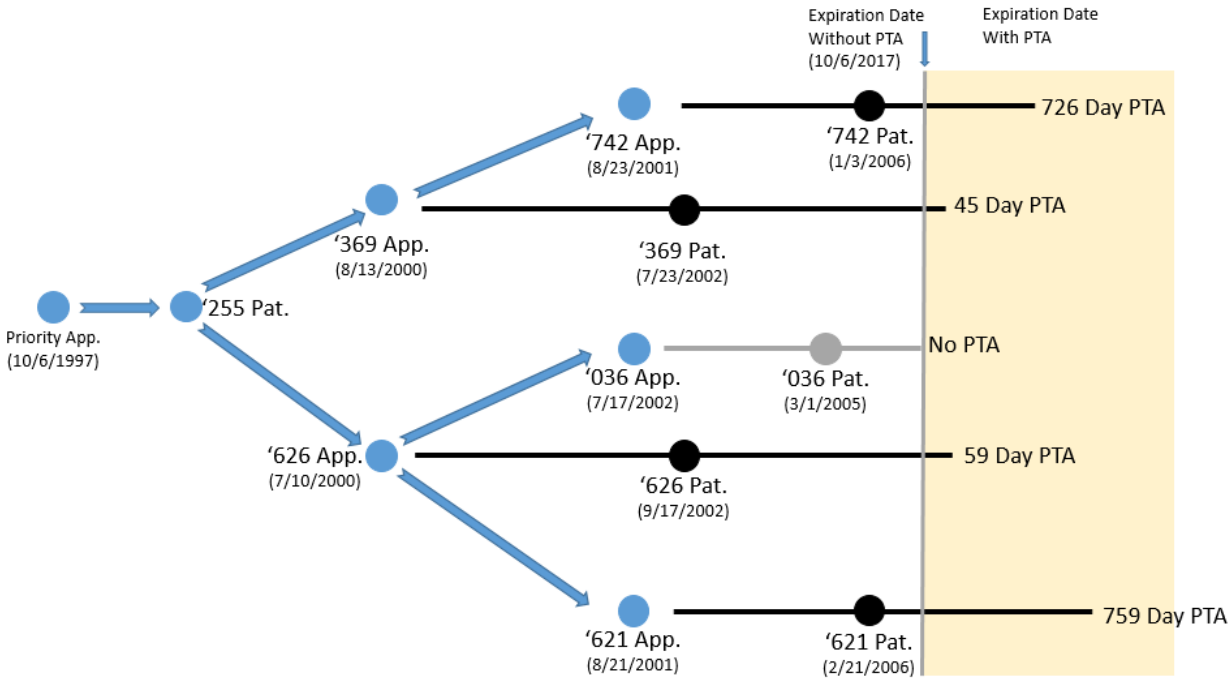
The Challenged Patents generally relate to “solid state image sensors,” with each Challenged Patent describing and distinctly claiming communication devices that are improved with reduced-area imaging devices (for example, solid state sensors that are of a minimum size). Appx132 (’742 Patent Abstract), Appx148 (’742 Patent at 1:20-26); Appx163 (’369 Patent Abstract), Appx177 (’369 Patent at 1:16-21); Appx189 (’626 Patent Abstract), Appx203 (’626 Patent at 1:15-21); Appx216 (’621 Patent Abstract); Appx232 (’621 Patent at 1:21-25).

In addition to having the same three inventors, all the Challenged Patents are assigned to the inventors’ family business, Cellect. Appx132, Appx163, Appx189, Appx216. Co-founder and Chief Technology Officer of Cellect and its parent company, Mr. Jeffrey Adair, pledged that Cellect will not assign these patents to another entity. Appx1745, Appx1753 (Mr. Adair’s declaration), ¶¶ 2, 24. The Challenged Patents are also part of the same patent family, all claiming priority to October 6, 1997, which is the filing of the parent application, U.S. Patent Appl. No. 08/944,322. Appx132, Appx163, Appx189, Appx216. In particular, the ’369

and ’626 Patents are continuations-in-part (“CIP”) of U.S. Patent No. 6,275,255 (“the ’255 Patent”), the ’742 Patent is a CIP of the ’369 Patent, and the ’621 Patent is a CIP of the ’626 Patent. *Id.*; *see also* Appx6549.

Between July 2000 and July 2002, Cellect filed the applications that matured into the Challenged Patents, along with U.S. Patent Appl. No. 10/198,189, which matured into the ’036 Patent. Appx132, Appx163, Appx189, Appx216, Appx6387 (the ’036 Patent). While there is no reexamination challenge to the ’036 Patent, the Board used the ’036 Patent (a continuation of the ’626 Patent) as a reference against the ’369 Patent. Appx28-29, Appx49 (Board’s ’369 Patent Decision).

As shown in the diagram below, due to Patent Office delays during prosecution, several of Cellect’s patents received a PTA pursuant to pre-AIA 35 U.S.C. § 154(b). The Patent Office calculated and granted the adjustments, which were included in the Notices of Allowance. Appx514-516 (’742 Patent); Appx998-1000 (’369 Patent); Appx6851-6853 (’626 Patent); Appx9715-9717 (’621 Patent). Notably, but for the PTAs, the Challenged Patents would have expired on the same day, October 6, 2017, which is the expiration of the unchallenged ’036 Patent that did not qualify for a PTA. Appx6387.



B. The Same Examiner Prosecuted the Applications of the Challenged Patents with the Requirements for Patentability in Mind

The same Examiner, Examiner Rao, evaluated all the patent applications of the Patents at Issue with all the members of the patent family in mind. Appx132, Appx163, Appx189, Appx216, Appx6387. The prosecution histories of the Cellect patents demonstrate that he was not only aware of the family relationships among these patents, but also understood and considered the relevancy of the related patent applications within the Cellect patent family during prosecution.

Examiner Rao conducted interference searches in accordance with the Manual of Patent Examining Procedure (June 2020) ("MPEP") § 2304.01(a), which requires that applications are searched against any other pending applications with conflicting claims. He recorded in the relevant prosecution

histories that he searched the correct classes for the Challenged Patents while examining the applications for the '742, '369, '626, and '621 Patents. Appx524-525 (interference search notes in classes 348, 382, and 455 from the '742 Patent file history); Appx1017 (interference search notes in classes 348 and 455 from the '369 Patent file history); Appx6880 (interference search notes in classes 348 and 455 from the '626 Patent file history); Appx9724 (interference search notes in classes 348 and 455 from the '621 Patent file history).

The unrebutted testimony of Mr. Robert Spar, the former Director of the Office of Patent Legal Administration and a 40-year veteran of the Patent Office (Appx2432-2435), confirmed that not only did Examiner Rao conduct the proper interference searches, but also that his searches demonstrated his consideration of any potential double patenting issues. Appx2439-2443 (Mr. Spar's declaration in the '742 Patent reexamination), ¶¶ 20, 29-33 (describing the interference search for the '742 Patent Application); Appx6247-6249 (Cellect's citation to and reliance on Mr. Spar's declaration submitted in the '626 Patent reexamination); Appx8108-8113 (Mr. Spar's declaration in the '626 Patent reexamination), ¶¶ 20, 28-32 (describing the interference search for the '369 and '626 Patent Applications); Appx10910-10915 (Mr. Spar's declaration in the '621 Patent reexamination), ¶¶ 20, 28-33 (describing the interference search for the '621 Patent Application). Mr.

Spar opined that this, along with other evidence of Examiner Rao's thoroughness during prosecution, shows that Examiner Rao considered double patenting. *Id.*

Further, Examiner Rao expressly acknowledged that he had considered related patents, including the parent patent applications that the Board now employs as double patenting references, during the prosecution of the applications for the '621 and '742 Patents. He signed his initials on an information disclosure statement ("IDS"), indicating he had considered the parent '626 Patent when evaluating its child '621 Patent Application. Appx9721 (initialed IDS from the '621 Patent file history, listing the '626 Patent); *see* MPEP § 609 (examiner initials on an IDS indicate information was considered). He also searched for the '626 Patent during prosecution of the '621 Patent, because he identified the application number for the '626 Patent in the list of search terms he used to look for prior art references. Appx9724 (search terms from the '621 Patent file history, identifying U.S. Patent Appl. No. 09/613,027, which matured into the '626 Patent).

While examining the patentability of the '621 Patent Application, Examiner Rao extended his evaluation beyond just the relevant parent patent. He also considered the '036 Patent. Appx9721 (initialed IDS from the '621 Patent file history, listing the '036 Patent). He used U.S. Patent Appl. No. 09/935,993, which matured into the '742 Patent, as another search term. Appx9724 (search terms from the '621 Patent file history). He even searched for and considered other

related patents within the same family but from earlier in the priority chain. *Id.* (search terms from the '621 Patent file history, identifying U.S. Patent Appl. No. 09/175,685, which matured into related U.S. Patent No. 6,043,839 ("the '839 Patent")); Appx9731-9732 (initialed IDS from the '621 Patent file history, listing related U.S. Patent No. 5,929,901 ("the '901 Patent")).

During prosecution of the '742 Patent application, he used the application number of its parent patent, the '369 Patent, in the list of search terms that he used to look for prior art references. Appx524 (search terms from the '742 Patent file history, identifying U.S. Patent Appl. No. 08/638,976, which matured into the '369 Patent). Again, he went beyond merely considering the parent application. He used additional related patents as search terms, such as U.S. Patent Appl. No. 09/934,201, which matured into the '621 Patent. *Id.* (search terms from the '742 Patent file history). He also initialed an IDS to show he considered the related '626 Patent, '036 Patent, and the earlier '901 Patent in connection with the '742 Patent prosecution. Appx531 (initialed IDS from the '742 Patent file history, listing the '626 and '036 Patents); Appx520 (initialed IDS from the '742 Patent file history, listing the '901 Patent).

Examiner Rao's search terms during prosecution also included the inventors' names. Appx524 (search terms from the '742 Patent file history), Appx9724 (search terms from the '621 Patent file history). That search would turn up the

parent patents and other related applications, as the Patents at Issue have the exact same inventors. Thus, he evaluated the child applications in light of their respective parents, as the MPEP requires. *See* MPEP § 609.02. Based on all the foregoing evidence, his thorough evaluations of Cellect's patent family extended not just ***down*** each parent-child line, but also ***across*** the various applications that followed the original priority application.

In addition, Examiner Rao considered the applicability of potential prior art across the family during prosecution. *See, e.g.*, Appx437-440, Appx947-953, Appx6785-6788, Appx9664-9667 (Office Actions for the '742, '369, '626, and '621 Patents, respectively). For example, he considered the same alleged prior art reference, Jacobsen *et al.*, in validity challenges to each of the Challenged Patents. *Id.* He also indicated that he considered the earlier '901 Patent in connection with his examination of the '369 Patent. Appx992 (initialed IDS from the '369 Patent file history, listing the '901 Patent).

There can be no reasonable dispute that Examiner Rao considered double patenting during the prosecution of the family of the Challenged Patents. Examiner Rao issued a double patenting rejection when warranted for the related '255 Patent application, which is the parent of the '626 and '369 Patents and the grandparent of the '742 and '621 Patents. Appx3259-3262 (Office Action based on double patenting for U.S. Appl. No. 09/496,312, which matured into

the ’255 Patent). He did not issue such a rejection in connection with the Challenged Patents because none was necessary.

C. The Board Affirmed the Patent Office’s Use of Patent Term Adjustments to Create Double Patenting References during Reexamination

The Board affirmed the Patent Office’s application of the judicially created doctrine of double patenting against the Challenged Patents based on certain patents’ statutorily granted PTAs, which resulted in each Challenged Patent expiring at a different time. Appx12-16, Appx35-38, Appx61-65, Appx84-89 (Board’s ’742, ’369, ’626, and ’621 Decisions, respectively, addressing applicability of double patenting to PTA). Specifically, the Patent Office relied on the adjusted expiration dates to create double patenting references and turn Cellect’s related patents against one another, even though Examiner Rao found no double patenting issues within this family during prosecution. Thus, the Patent Office weaponized the following patents against their term-adjusted relatives:

- The ’369 Patent allegedly invalidates its own child, the ’742 Patent. Appx24. The ’369 Patent is the earlier-filed and earlier-issued patent.
- The ’626 Patent allegedly invalidates its own child, the ’621 Patent. Appx97. The ’626 Patent is the earlier-filed and earlier-issued patent.
- The ’036 Patent allegedly invalidates the related ’369 Patent. Appx49. The ’036 Patent is the later-filed and later-issued patent.

- The ’369 Patent allegedly invalidates the related ’626 Patent. Appx73. The ’369 Patent is the later-filed and earlier-issued patent.

In affirming the Patent Office’s decision, the Board also summarily concluded that double patenting applies to the ’742, ’626, and ’621 Patents ***regardless*** of the PTAs. Appx18-19, Appx67-68, Appx91-92 (’742, ’626, and ’621 Decisions, respectively). It based this argument on the Patent Office’s conclusory statement that “regardless whether two relevant patents have different expirations,” double patenting may apply. Appx4112 (Examiner’s Answer in reexamination of the ’742 Patent), Appx9233-9234 (Examiner’s Answer in reexamination of the ’626 Patent). But the Board never explained why this position applies in this case, where there is no gamesmanship and no risk of divided ownership.

SUMMARY OF ARGUMENT

The judicially created doctrine of obviousness-type double patenting simply does not apply to Cellect’s Challenged Patents, because they are related and would have expired on the same day but for receiving PTAs pursuant to 35 U.S.C. § 154(b). The Board legally erred by forcing application of double patenting based solely on the PTAs in and of themselves. In so doing, the Board treated PTAs pursuant to 35 U.S.C. § 154(b) differently from PTEs pursuant to 35 U.S.C. § 156 for purposes of double patenting, which is illogical and contrary to law and

Congressional intent. This Court has found that an extension does not transform a patent into a double patenting reference because the "judge-made doctrine" of double patenting cannot "cut off a statutorily-authorized time extension," and it should find the same with respect to adjustments because they are simply another form of "statutorily-authorized time extension." *Novartis*, 909 F.3d at 1375. The Board should have followed this Court's precedent.

Double patenting exists to prevent two equitable considerations, neither of which are present here: an unjust timewise extension of patent term through manipulative prosecution, and harassing litigation filed by multiple patent owners that split multiple patents for the same invention between them. MPEP § 804. Here, there is no allegation that Cellect engaged in gamesmanship or crafty prosecution to secure extra patent term. Indeed, Cellect received the statutorily mandated adjustments because of Patent Office delays during prosecution, through no fault of Cellect. Any alleged risk of claim splitting is entirely speculative, particularly given that Cellect's Chief Technology Officer affirmed that Cellect has always and will always keep the Challenged Patents. Appx1753 (Adair Decl.), ¶ 24. Thus, the Challenged Patents do not trigger either of the traditional concerns that might warrant application of double patenting.

No substantial new question of patentability exists in this case that could justify reexamination of Cellect's related patents. The same examiner evaluated

Cellect's Patents at Issue, all of which have the same inventors. He considered the applications in light of the other related patents, and did not issue a double patenting rejection because one was not warranted. In contrast, he ***did*** issue a double patenting rejection when warranted against another application in the same patent family. Appx3258-3262 (Office Action for the '255 Patent). The Board cannot create a substantial new question of patentability by second-guessing the examiner's judgment. Nor does the PTA, in and of itself, shed "new light" on patentability, because the original examiner of the Challenged Patents knew of the adjustments and how long they would be during prosecution. 37 C.F.R. § 1.705 (pre-2013-04-01) (requiring that Patent Office identify adjustments with the Notice of Allowance).

The Board's Decisions deploy an equitable doctrine to achieve an inequitable result—namely, to punish Cellect for its indisputably proper, statutorily granted term adjustment. Even if this Court permits this retroactive creation of double patenting references out of related patents, only the adjustment should be invalidated—not the patent.

The Board's only remaining invalidity allegations depend on double patenting in combination with alleged 35 U.S.C. § 103 references. Since double patenting is inappropriate here, these allegations also fail.

ARGUMENT

I. STANDARD OF REVIEW

This Court reviews *de novo* the Board's erroneous statutory interpretation causing patents with statutorily granted adjustments to be treated differently than patents with statutorily granted extensions for purposes of obviousness-type double patenting. 5 U.S.C. § 706 (the court reviewing an agency action "shall decide all relevant questions of law [and] interpret [] statutory provisions"); *see also In re Vivint, Inc.*, 14 F.4th 1342, 1348 (Fed. Cir. 2021) (subjecting the Board's inconsistent treatment of a similar issue appearing in two statutory frameworks to plenary review).

The Board's decision that a PTA based on Patent Office delays, without more, creates a substantial new question of patentability is also a question of law "review[ed] without deference." *In re Vivint*, 14 F.4th at 1348. "As with statutory obviousness under 35 U.S.C. § 103, obviousness-type double patenting is an issue of law premised on underlying factual inquiries." *Eli Lilly & Co. v. Teva Parenteral Meds., Inc.*, 689 F.3d 1368, 1376 (Fed. Cir. 2012) (citation omitted). This Court "review[s] the Board's ultimate determination of obviousness de novo and the Board's underlying factual findings for substantial evidence." *In re Glatt Air Techniques, Inc.*, 630 F.3d 1026, 1029 (Fed. Cir. 2011) (finding that the Board

failed to make a proper prima facie case for obviousness because substantial evidence did not support the Board's findings) (citation omitted).

II. THE BOARD LEGALLY ERRED IN TREATING PATENT TERM ADJUSTMENTS DIFFERENTLY THAN PATENT TERM EXTENSIONS FOR PURPOSES OF DOUBLE PATENTING

A. Patent Term Restoration Based on Government Delays Should Be Treated the Same

The Board misinterpreted and ignored this Court's guidance in *Novartis* and *Merck* when it affirmed the use of the judge-made, non-statutory doctrine of double patenting to invalidate patents solely because the patent terms were extended under 35 U.S.C. § 154(b). *Novartis*, 909 F.3d at 1372-75; *Merck & Co. v. Hi-Tech Pharmacal Co.*, 482 F.3d 1317, 1322 (Fed. Cir. 2007). This Court has held that double patenting cannot "cut off a statutorily-authorized time extension." *Novartis*, 909 F.3d at 1375. The Board ignored this guidance and distinguished PTA from PTE using a rationale that is both legally flawed and internally inconsistent.

The Board committed legal error in determining that it should treat PTA and PTE differently for purposes of double patenting. Two statutory frameworks accomplish the goal of Congress to "restore the value of the patent term that a patent owner loses during the early years of the patent . . . ." *Novartis*, 909 F.3d at 1369; *see also* H.R. Rep. 106-287(I) (1999) at 49-50. Congress intended both patent term extensions (35 U.S.C. § 156) and patent term adjustments (35 U.S.C. §

154(b)) to be statutory "technical term adjustment provisions" that restore patent term lost to different types of administrative delay. *See* H.R. Rep. 106-287(I) (1999) at 51 ("coordinat[ing]" adjustments and extensions). Given the parallels between the two types of patent term restoration, adjustments should be treated the same as extensions when government delays, as opposed to any activities of the patent applicant, is the basis for the adjustment.

The Congressional intent behind these doctrines emphasizes this very point. As part of the Hatch-Waxman Act in 1984, patents covering subject matter that requires regulatory review, like pharmaceutical patents, "shall be extended" up to five years, upon patent owner's application and the satisfaction of various conditions. *See* 35 U.S.C. §§ 156(c), 156(g)(6). In 1999, Congress provided that a patent for any subject matter "shall be extended" one day for each day of delay in prosecution that is attributable solely to the Patent Office, through no fault of the patent owner. 35 U.S.C. § 154(b)(1)(A).

Each statute also identifies certain limitations on its applicability. For example, a patent owner must choose only one patent for a § 156 extension if there are multiple patents involved in the same regulatory review period for a given product. 35 U.S.C. § 156(c)(4). For § 154 adjustments, the length of the term adjustment cannot cause the patent's term to exceed the expiration date specified in a terminal disclaimer. 35 U.S.C. § 154(b)(2)(B).

The Board's inconsistent application of the statutory framework and how it applies to double patenting cannot be reconciled with the foregoing Congressional intent and this Court's precedent. Given the parallels, PTAs and PTEs should be treated consistently when applying the judicially created doctrine of double patenting. It cannot be, as the Board erroneously concluded, that adjustments—but not extensions—can transform a related patent into a double patenting reference. That, however, was precisely what the Board did here—it used related patents to invalidate Cellect's Challenged Patents. This creates a tension in the law that defies common sense. In refusing to follow this Court's reasoning in *Novartis*, which addressed PTEs, the Board attempts to make new law drawing an artificial distinction between PTE and PTA as they relate to double patenting.

In *Novartis*, this Court interpreted 35 U.S.C. § 156 and found that the plain meaning of the statute did not reflect additional limitations that defendant Ezra proposed were necessary to combat alleged double patenting violations. *Novartis*, 909 F.3d at 1372-73. The Court further held that a patent is not at risk of invalidation for double patenting just because "the term extension it received causes the [extended] patent to expire after [another] allegedly patentably indistinct [] patent." *Id.* at 1373. Here, consistent with *Novartis*, the plain meaning of § 154(b) should control and a patent should not be at risk of invalidation for double

patenting just because it received a term ***adjustment*** that causes it to expire after another allegedly patentably indistinct patent.

Moreover, as this Court has observed, the "judge-made doctrine" of double patenting should not "cut off a statutorily-authorized time extension," because the entire point of the doctrine was to "prevent extension of a patent beyond a '***statutory*** time limit.'"[2] *Novartis*, 909 F.3d at 1375 (emphasis added) (citation omitted). Such a consideration applies equally to both types of term restoration because they are both statutory time limit modifications for patent term. This Court's guidance in *Novartis* should apply here to avoid the inconsistencies that arise from the Board's contrary interpretation.[3] Thus, the Board's legal error requires reversal.

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[2] The Board claims this Court already decided PTAs could create double patenting issues, but this Court's observation that statutory restoration could affect expiration dates ***predates*** the *Novartis* decision on how to actually handle such patent term restorations. *See* Appx15, Appx38, Appx64, Appx88-89 (all citing *Abbvie Inc. v. Mathilda & Terence Kennedy Institute of Rheumatology Trust*, 764 F.3d 1366, 1373 (Fed. Cir. 2014)). In fact, this Court distinguished *AbbVie* in *Novartis* because a patent term extension raised "no concern that [patent owner], once its [] patent issued, sought to subsequently 'secur[e] a second, later expiring patent for the same invention,' as in *AbbVie* . . . ." 909 F.3d at 1375 (quoting *Abbvie*, 764 F.3d at 1373).

[3] The Board wrongly claims that Cellect would apply different dates for purposes of determining terminal disclaimers than for double patenting, without citation. Appx16, Appx38, Appx65, Appx89. Cellect made no such argument. In line with *Novartis*, the double patenting analysis should compare original expiration dates when the sole reason that expiration dates differ is a statutory restoration of patent term. It is unclear to what contradictory positions the Board refers.

B. The Plain Language of 35 U.S.C. § 154(b) Forecloses the Board's Claim that Patent Term Adjustments by Themselves Create Double Patenting Issues

The Board does not dispute that Cellect's Challenged Patents were entitled to and received properly calculated term adjustments based on Patent Office delay. As a "[g]uarantee of prompt patent and trademark office responses . . . if the issue of an original patent is delayed due to the failure of the [Patent Office]" to adhere to certain deadlines for timely prosecution, then "the term of the patent ***shall*** be extended 1 day for each day" of delay. *Compare* 35 U.S.C. § 154(b)(1)(A) *with* 35 U.S.C. § 156(c) ("[t]he term of a patent eligible for extension . . . ***shall*** be extended by the time equal to the regulatory review period for the approved product . . .") (all emphases added); *Novartis*, 909 F.3d at 1372 (acknowledging purpose of statutory frameworks). "Use of the word 'shall' in a statute generally denotes the imperative." *Merck*, 482 F.3d at 1322 (interpreting § 156) (citations omitted). Thus, the Patent Office granted Cellect the appropriate PTAs by statutory mandate.

But the Board heavily relied upon the following portion of § 154(b), which is the exception to the mandatory term adjustment:

> No patent the term of which has been disclaimed beyond a specified date may be adjusted under this section beyond the expiration date specified in the disclaimer.

35 U.S.C. § 154(b)(2)(B). This exception in the statute, however, addresses an existing terminal disclaimer made during the prosecution of a patent application.

The Board rewrites this portion of the statute to support its argument that the adjustment itself creates a double patenting issue, which is erroneous because the statute says nothing about double patenting.

The Board's statutory interpretation would effectively eviscerate § 154(b) as it would make adjustments unavailable to related patents, because such adjustments would also invalidate them. *See* Appx12-16, Appx35-38, Appx61-65, Appx86-89. The only way to guarantee that a patent owner avoids the unreasonable result visited on Cellect would be to file a preemptive terminal disclaimer with every continuation patent. Without such a disclaimer, any adjustment could create a double patenting issue amongst related patents where one never existed before. But with such a disclaimer, continuation patents could never receive an adjustment to offset Patent Office delays that diminished the patent owner's rightful term. 35 U.S.C. § 154(b)(2)(B) (patents with terminal disclaimers cannot receive an adjustment that recaptures disclaimed term). The Board's decision not only uses a judicially created doctrine to cut off a statutorily mandated time extension; it uses a judicially created doctrine to eliminate Congress' compensation to patent owners for administrative delays that interfere with the foundational *quid pro quo* of patent law. The fact that a comparable statutory provision for term extensions is treated entirely differently only compounds the legal error.

The Board's position is contrary to principles of statutory interpretation. The plain meaning of this limitation on a "patent the term of which has been disclaimed" is exactly as it sounds—a limitation on a patent with an existing disclaimer, not a "patent the term of which [may need to be] disclaimed [if adjustment is granted]." *See Novartis*, 909 F.3d at 1372 (citation omitted) ("[C]ourts 'ordinarily resist[] reading words into a statute that do not appear on its face.'"). Section 154(b)(2)(B) is unambiguous that it applies to ***existing*** disclaimers. Since none of the Challenged Patents has a terminal disclaimer, the exception is inapplicable on its face.

Nothing in the plain meaning of § 154(b)(2)(B) or the Congressional intent behind it demonstrates that Congress intended for the Patent Office to check if the adjustment would result in a patent needing a ***new*** terminal disclaimer based on the adjustment itself. Congress enacted §§ 156 and 154(b) to accomplish similar goals. *See Merck*, 482 F.3d at 1322 (affirming validity of extension and discussing Congressional intent). Nor does the contrast between the limitations on extensions and the limitations on adjustments somehow make § 154(b)(2)(B) applicable. The Board seeks to broaden § 154(b)(2)(B) to force its application here, but this is an improper attempt to inject extra-textual limitations into an unambiguous statute. When statutory conditions are met, the patent term "***shall*** be extended" to account for delay, provided that the adjustment does not seek to reclaim any patent term

that "has been disclaimed beyond a specified date." *See* 35 U.S.C. § 154(b) (emphasis added).

The surrounding statutory text supports Cellect's straightforward reading. The most natural reading of a "specified date" and an "expiration date specified in the disclaimer" is a date already specified in a disclaimer already made. No conditional language exists indicating that even for patents the term of which has ***not*** been disclaimed, such a patent should only receive adjustment after considering if the adjustment itself could make a disclaimer applicable.[4]

The Board misconstrued the meaning of "terminal disclaimer" to shoehorn this nonexistent conditional language into § 154(b)(2)(B). It contended that "given that terminal disclaimers arise ***almost*** exclusively to overcome obviousness-type double patenting, Congress expressly addressing terminal disclaimers in § 154 ***is tantamount to addressing*** obviousness-type double patenting." Appx14, Appx37, Appx63, Appx87 (Board's Decisions) (emphases added) (citations omitted). The Board thus concluded that rather than simply stating that a PTA cannot restore already-disclaimed patent term, the statute ***also states*** that any adjusted patent

[4] The Board notes that the Director has discretion to "establish[] procedures for the application for and determination of patent term adjustments," but declines to consider "whether that discretion includes the [adjustment] issues here." Appx16 n.6, Appx38-39 n.5, Appx65 n.6, Appx89 n.5 (Board's Decisions, citing 35 U.S.C. § 154(b)(3)(A)). In other words, the Board ignored whether any established Patent Office procedures obviate the Board's concerns or contradict its position.

should undergo a double patenting analysis against any related patents using the date of the adjustment—regardless of whether any double patenting issues existed before adjustment.

This interpretation is legal error for at least three reasons. First, the Board failed to identify any ambiguity justifying its reconstruction of the statute, because there is none. The most natural reading controls. *Merck*, 482 F.3d at 1322. Second, the Board recasts the words that Congress ***actually*** chose because, in the Board's view, they are "tantamount to" using different terminology requiring consideration of a judicially created test. It offered no support in the statutory text (or legislative history) that Congress intended to incorporate the judicial doctrine of double patenting into its statutory mandate or intended to create grounds for a ***new*** double patenting analysis.[5] Third, the Board notes that terminal disclaimers may sometimes arise independently of double patenting, but it apparently does not seek to read these circumstances into the statute—a choice that injects ambiguity into an otherwise clear statutory framework. The Board's selective redefinition of what is an existing disclaimer raises a red flag, signaling departure from the plain meaning of the statute.

[5] And even if this Court does read the statute in the manner the Board suggests, the attack should be on the validity of the adjustment—not the patent. *See infra*, Section V.

Cellect's straightforward textual reading of §§ 154(b) and 154(b)(2)(B) also aligns with this Court's guidance in *Novartis*. In that case, this Court examined one of the statutory limitations on the scope of patent term extensions under § 156. *Novartis*, 909 F.3d at 1373. Section 156(c)(4) limits a patent owner's application for extension to just one patent per covered product, stating that "in no event shall more than one patent be extended . . . ." 35 U.S.C. § 156(c)(4). Defendant Ezra claimed this Court should read § 156(c)(4) to ***also*** mean that no more than one patent could be "effectively extended," arguing that a patent with a terminal disclaimer should not be extended lest any patentably indistinct variants "effectively" also receive extra term. *Novartis*, 909 F.3d at 1372-73. The Court declined Ezra's invitation to broaden the scope of the limitation on extensions beyond its plain meaning, noting in particular that Congress did not write "effectively" in the statute. *Id*.

Similarly, here, this Court is evaluating one of the statutory limitations on the scope of patent term adjustments. The Board seeks to expand the scope of the statutory limitation on terminally disclaimed patents to also limit patents without existing disclaimers, using the adjustment itself as the invalidating basis. As in *Novartis* and *Merck*, this Court should reject these arguments because they do not comply with basic principles of statutory interpretation. The Board's insistence that this provision nonetheless applies to the Challenged Patents without terminal

disclaimers "ignores the word 'shall'" and fails to apply "the most natural reading of the statutory language." *See Merck*, 482 F.3d at 1322 (declining to read in a limitation on availability of an extension that lacked support in statutory text); *Novartis*, 909 F.3d at 1372-73 (declining to read extended in statutory limitation to also mean "effectively extended," which would broaden application of statutory limitation beyond plain meaning).

Cellect's non-terminally disclaimed patents are entitled to their periods of adjustment, and those adjustments have nothing to do with a double patenting analysis. Section 154(b)(2)(B) does not say otherwise.

C. District Courts Have Applied this Court's Holding in *Novartis* to Patent Term Adjustments

Two District Courts have addressed how PTA intersects with double patenting in light of *Novartis* and determined that PTA must be treated the same way as PTE with respect to double patenting. In *Mitsubishi*, the Chief Judge of the District Court of New Jersey, applying *Novartis,* came to this conclusion. *Mitsubishi Tanabe Pharma Corp. v. Sandoz Inc.*, 533 F. Supp. 3d 170 (D.N.J. 2021). The District Court recognized that "[t]he Federal Circuit has not, however, had occasion to consider the instant situation: whether a later-filed, later-issued patent that expires before the earlier-filed, earlier-issued patent due to a statutorily allowed term extension under § 154(b), can act as an obviousness-type double patenting reference." *Id*. at 213. Then the *Mitsubishi* court evaluated the same key

facts present in this case—two patents in the same patent family would have expired on the same date but for the fact that one received a indisputably proper patent term adjustment pursuant to § 154(b). *Id.* at 213-14.

The District Court reviewed this Court's guidance on double patenting from *Gilead* through *Novartis* and determined that "the granting of a [patent term adjustment] does not present the potential for gamesmanship by inventors to secure a second, later-expiring patent for the same invention." *Id.* at 214; *see also Gilead Scis., Inc. v. Natco Pharma Ltd.*, 753 F.3d 1208, 1210, 1217 (Fed. Cir. 2014) (later-issued but earlier-expiring patent could be double patenting reference against unrelated patent). As the District Court emphasized, "[p]erhaps more importantly, however, the Court is swayed by the Federal Circuit's observation that 'a judge made doctrine' should not be used to 'cut off a statutorily-authorized time extension.'" *Mitsubishi*, 533 F. Supp. 3d at 214 (citing *Novartis,* 909 F.3d at 1375). The *Mitsubishi* court concluded, "[a]greeing with [defendant's] position would mean just that," (*i.e.*, cutting off a statutorily authorized time extension). *Mitsubishi*, 533 F. Supp. 3d at 214. Agreeing with the Board's position in this case would mean "just that" as well.

The Board attempted to distinguish the *Mitsubishi* decision, showing much disrespect to both the Court's analysis and an Article III judge. *See, e.g.*, Appx17, Appx40, Appx66-67, Appx90-91 (Board's Decisions, stating "[T]he court does not

appear to have understood that a terminal disclaimer is the standard way to cure double patenting, . . .” and concluding that “it is not clear whether the district court was even considering the right facts.”). The Board gave “little weight” to the *Mitsubishi* decision because of four stated reasons.

First, the Board cites to *Magna* as a case that “came out the opposite way from *Mitsubishi*.” Appx16, Appx39, Appx66, Appx90 (Board’s Decisions, citing *Magna Elecs., Inc. v. TRW Automotive Holdings Corp.*, Nos. 1:12-cv-654, 1:13-cv-324, 2015 WL 11430786 (W.D. Mich. Dec. 10, 2015)). What the Board fails to appreciate is that *Magna* was decided prior to this Court’s decision in *Novartis* and thus could not apply its precedential analysis regarding statutory term extensions. Additionally, the Board fails to recognize the distinct factual differences between this case and *Magna*. For example, *Magna* involved patents examined by ***different*** examiners during original prosecution, such that it was “not even clear that the primary examiner was aware of the [other patent’s] claims.” *Magna*, 2015 WL 11430786, at *3. The reasoning in *Magna* lacked this Court’s guidance on other types of term restoration and is not applicable here where one examiner was involved in the prosecution of all the Patents at Issue and demonstrated he was well-aware of Cellect’s applications and patent family.

Second, the Board faults the District Court for failing to address the fact that double patenting can apply “even to two patents that have the same filing date, the

same issue date, and the same expiration date" because it may be "needed to ensure that two patents remain commonly owned." Appx17, Appx39, Appx66, Appx90 (Board's Decisions, citing *Underwood v. Gerber*, 149 U.S. 224 (1893); *Sandy MacGregor Co. v. Vaco Grip Co.*, 2 F.2d 655, 657 (6th Cir. 1924)). While the Board later argues that such gamesmanship is not necessary to apply the doctrine of double patenting, it does not make sense to punitively apply an equitable doctrine designed to prevent gamesmanship where gamesmanship does not exist, as the *Mitsubishi* court reasoned. *Compare Mitsubishi*, 533 F. Supp. 3d at 214 *with*, *e.g.*, Appx20, Appx45-46, Appx69-70, Appx93-94 (Board's Decisions); *see also* H.R. Rep. 106-287(I) (1999) at 48-49 (any § 154(b) adjustment is offset by any days of applicant-caused delay, punishing only those that "purposely manipulate" system). Thus, the Board's criticism of the District Court's analysis regarding potential gamesmanship is a red herring because the District Court already determined there was none.

Third, the Board states that the District Court does not understand the law regarding terminal disclaimers, "thereby overlooking why the Federal Circuit decided a rule for terminal disclaimers (*Merck v. Hi-Tech*) should also apply to a double patenting analysis (*Novartis v. Ezra*) as a 'logical extension.'" Appx17, Appx40, Appx66-67, Appx90 (Board's Decisions, citing *Mitsubishi*, 533 F. Supp. 3d at 214 n.45). The Board repeatedly emphasizes this Court's observation that its

Novartis holding is a "logical extension" of its *Merck* holding and thus adjustments and extensions cannot be treated consistently, when in fact the "logical extension" argument supports application of the *Novartis* reasoning here. *See* Appx11, Appx14-15, Appx17 (Board's '742 Decision relying heavily on "logical extension" argument); Appx34, Appx37, Appx40 (same for the Board's '369 Decision); Appx60, Appx63-64, Appx66-67 (same for the Board's '626 Decision); Appx84-85, Appx88, Appx90 (same for the Board's '621 Decision).

In context, this Court wrote, "[w]e conclude, as a logical extension of our holding in [*Merck*], that obviousness-type double patenting does not invalidate a validly obtained [extension] in such a scenario," where the scenario is "the term extension it received causes the [] patent to expire after [an] allegedly patentably indistinct [] patent." 909 F.3d at 1373; *see also id.* at 1369 (the only other mention of "logical extension," in substantially the same sentence). The Board's heavy reliance appears misplaced, as it seems unlikely this Court was signaling anything about the substance of § 154 by observing that *Novartis* is logical in light of *Merck*. Nonetheless, it is perfectly logical that where a validly obtained statutory term restoration exists (*Merck*), it follows that such a restoration cannot, without more, become the basis for invalidation for double patenting (*Novartis*).

Fourth, the Board gave little weight to the *Mitsubishi* decision because it alleges "it is not clear whether the district court was even considering the right

facts." Appx17, Appx40, Appx67, Appx91. A simple read of the decision, however, demonstrates that the Chief Judge of the District Court of New Jersey had extensive knowledge of the facts of the case and applied them to the precedent provided by this Court with respect to PTE and double patenting. In the paragraph the Board criticizes, the District Court (1) explained that in ***its*** case, but for the PTA, the alleged reference and the challenged patent would expire at the same time (citing the factual record); (2) distinguished the *Gilead* case involving unrelated patents expiring at different times; and (3) concluded that "[i]n ***that*** connection," *i.e.*, to match the facts of *Gilead* just discussed, the alleged reference patent "would have expired before" the challenged patent but for the PTA (citing this Court's precedent, not the factual record). *Mitsubishi*, 533 F. Supp. 3d at 214 (emphasis added). This Court should rebuke the Board's disregard of the *Mitsubishi* decision based on specious claims that the District Court did not know the facts of its case.

Another judge in the District of New Jersey evaluated this term restoration issue in detail and came to the same conclusion as the Chief Judge in *Mitsubishi*. *Amgen*, 2021 WL 5366800, at *26-27. The District Court relied on *Novartis* to hold that both types of restoration should be treated the same: "[a] difference in expiration dates between two patents that arises solely from a statutorily authorized time extension, such as a patent-term adjustment pursuant to 35 U.S.C. § 154(b) or

a patent-term extension pursuant to 35 U.S.C. § 156, cannot be the basis for an application of [double patenting]." *Id.* at *26 (citing, *inter alia*, *Novartis*, 909 F.3d at 1372-75). The District Court further determined that "[e]ven if the '283 Patent were a proper [double patenting] reference for the '638 Patent, the Court would exercise its equitable discretion not to apply the doctrine of [double patenting] under the circumstances of this case because the difference in expiration dates between the '638 and '283 Patents is not the result of prosecution gamesmanship or any improper conduct by Celgene." *Amgen*, 2021 WL 5366800, at *27 (citing *Immunex Corp. v. Sandoz, Inc.*, 964 F.3d 1049, 1059 (Fed. Cir. 2020) (noting that double patenting is an "equitable doctrine"); *Novartis Pharm. Corp. v. Breckenridge Pharm., Inc.*, 909 F.3d 1355, 1364 (Fed. Cir. 2018) (declining to apply double patenting when "happenstance of an intervening change in patent term law" caused difference in expiration dates, rather than "prosecution gamesmanship"); *Gilead*, 753 F.3d at 1210 (double patenting applies when patent owner structured priority claims to achieve extra term)) (further citation omitted). As in *Amgen*, the Patent Office has made no claims of gamesmanship against Cellect in this case.

In both instances post-*Novartis* where District Courts determined the applicability of double patenting in view of a PTA, they followed this Court's guidance and determined that § 154(b) should be treated the same as § 156 with

respect to double patenting. Consistent treatment of these two statutory frameworks is the most logical and legally correct statutory interpretation—the Board got it wrong, and the two District Courts got it right.

D. The Board's Differential Treatment of Extensions and Adjustments Is Illogical and Unworkable

That § 156 and § 154 each have their own limitations on when to issue mandatory time extensions does not justify the Board's proposed disparate treatment for purposes of double patenting. The Board baselessly assumes that because the statutes treat terminally disclaimed patents differently, as described *supra* Section II(A)-(B), this case involving a post-prosecution double patenting objection against patents with adjustments (but without terminal disclaimers) must somehow come out opposite to this Court's treatment of the same objection to patents with extensions (and with terminal disclaimers). *See, e.g.*, Appx13-14, Appx36-37, Appx62-63, Appx86-87 (Board's Decisions, concluding "the rule" in *Merck* and *Novartis* "does not apply to a[n] [adjustment] because those decisions were premised on the contrast between [adjustments] and [extensions]").

Such an assumption is legal error. First, it is contrary to the plain language of § 154(b), as explained *supra*, Section II(A)-(B). The Board identified no reason to interpret a statutory provision about terminal disclaimers as a Congressional proxy for how and when to conduct a double patenting analysis. Second, it is contrary to Congressional intent. Congress describes both statutes as "technical

term adjustment provisions" and intentionally "coordinated" the two to clarify that any extension "shall include" any adjustment. H.R. Rep. 106-287(I) (1999) at 51; 35 U.S.C. § 156(a). Third, the Board's interpretation causes conflict with § 156(a), highlighting its lack of foundation in any statutory text or Congressional intent.

In practice, the Patent Office could not apply the Board's proposed distinction between extensions and adjustments without creating inconsistencies. For example, when a patent has both an extension and adjustment, using the "final" adjusted and extended expiration date erases the distinction the Board seeks to draw here by treating the extension and adjustment in the same manner for purposes of double patenting. Further, that approach violates the principle set forth in *Novartis* because it uses the extension as a basis for double patenting. But basing the expiration date solely on either the extension or the adjustment artificially ignores the existence of the other type of time extension.

As explained in detail *infra*, Section III, patent term restoration provisions like adjustments and extensions do not trigger the concerns that the judiciary created the double patenting doctrine to address—namely, unjust timewise extensions and litigation harassment. Use of an artificial expiration date for purposes of double patenting also does not serve these goals, because it does not reflect a patent term that the patent owner will actually receive. There is no way to

consider the justice of a time extension that does not reflect the actual amount of time received.

In contrast, if both statutes are treated consistently like the "technical term adjustment provisions" that they are, which do not of themselves create double patenting issues, then the composition of a term restoration is irrelevant. *See* H.R. Rep. 106-287(I) (1999) at 51; *cf. Amgen*, 2021 WL 5366800, at *26-27 (when following *Novartis*, it was irrelevant that the alleged reference patent had both an extension and adjustment). The original expiration date of the patent would control for purposes of double patenting.

III. THE EQUITABLE CONCERNS UNDERPINNING THE DOUBLE PATENTING DOCTRINE DO NOT EXIST IN THIS CASE

The Patents at Issue—which are all related—do not implicate the concerns that the judiciary sought to mitigate when it created the doctrine of double patenting. MPEP § 804 notes:

> Where the claims of an application are not the 'same' as those of a first patent, but the grant of a patent with the claims in the application ***would unjustly extend the rights*** granted by the first patent, a double patenting rejection under nonstatutory grounds is proper. . . . A rejection based on nonstatutory double patenting is based on a judicially created doctrine grounded in public policy so as to prevent the unjustified or improper timewise extension of the right to exclude granted by a patent. . . . A double patenting rejection also serves public policy interests by preventing the possibility of multiple suits against an accused infringer by different assignees of patents claiming patentably indistinct variations of the same invention.

MPEP § 804 (emphasis added) (citations omitted). A double patenting rejection is thus proper where the patent rights would ***unjustly*** extend the rights of a first patent. This unjust extension would occur under one of the two underlying policy grounds—improper timewise extension or harassment by multiple assignees—neither of which is present here.

When Congress created the PTA, they referred to it as a tool to "guarantee" the patent term to which a patent owner is entitled. H.R. Rep. 106-287(I) (1999) at 48-49. They intended to "compensate patent applicants for certain reductions in patent term that are not the fault of the applicant," particularly because previously "no adjustments were provided for administrative delays caused by the PTO that were beyond the control of the applicant." *Id.* Congress observed:

> [N]o patent applicant diligently seeking to obtain a patent will receive a term of less than the [statutory number of] years . . . ***Only*** those who ***purposely manipulate*** the system to delay the issuance of their patents will be penalized under [this title], a result that the Committee believes entirely appropriate.

Id. at 49 (emphasis added). The Board has not and cannot point to any evidence that Cellect has "purposely manipulate[d] the system to delay the issuance" of the Challenged Patents and improperly extend their term. To penalize a "diligent" applicant using the very provision intended to "guarantee" patents their proper term is inequitable and contrary to Congressional intent.

Here, Cellect did not devise a pattern of patent filings that would have required a terminal disclaimer. *See Novartis*, 909 F.3d at 1374 (distinguishing *Gilead* because that case involved "potential gamesmanship [] through structuring of priority claims"); *see also Gilead*, 753 F.3d at 1210 (patents covering same invention were ***unrelated***). Cellect's patents are all ***related***. Because of their relationship, they all originally expired on the same date. Thus, under their pre-adjustment shared expiration date, not only were they "valid under all other provisions of law" (*Novartis*, 909 F.3d at 1374), but they also showed no sign of the gamesmanship that double patenting prevents. There is nothing untoward in permitting Cellect the benefit of the adjustment.

This Court has emphasized the importance of the specific facts of a case when the mere operation of a statutory change in patent term is alleged to create double patenting issues, and thus this Court should weigh heavily the relationship amongst Cellect's patents. *See, e.g.*, *Novartis*, 909 F.3d at 1375 ("[b]ut for" the § 156 extension, challenged patent would have expired before the alleged reference, so there was "no concern" that patent owner sought a "second, later-expiring patent for the same invention"); *Breckenridge*, 909 F.3d at 1367 (but for intervening change in law governing length of patent term, challenged patent would have expired before alleged reference, so use as a reference was improper); *Amgen*, 2021 WL 5366800, at *27 (even if adjustments should create basis for

double patenting, lack of gamesmanship indicates inappropriateness of applying double patenting doctrine). Here, the Patents at Issue are ***all*** related with the same shared priority claim and the same expiration date, but for the term adjustments.

The Board relies on a case from 1893, *Underwood v. Gerber*, to support its argument that a patent expiring on the same day as another patent may nonetheless invalidate it. Appx17-18, Appx39, Appx66, Appx68, Appx90. In that case, the patent owner applied for two indistinct patents on the same day and asserted only one of the two in an infringement litigation, reserving the other. *Underwood*, 149 U.S. at 224, 227. The defendant raised the reserved patent as prior art which the Supreme Court confirmed rendered the first obvious. *Id.* at 227-31. This extreme fact pattern is far afield from Cellect's valid continuation practice protecting the various aspects of its inventions, with an examiner that considered other related applications. Further, Cellect has never and will never split its patents amongst multiple owners, nor has it. Appx1753 (Adair Decl.), ¶ 24. Thus, the risk of claim splitting or harassment by multiple litigants is entirely speculative.

This Court should not endorse the Board's use of double patenting to summarily invalidate related patents with shared expiration dates, based on a "risk" of divided ownership of ***related*** patents that is nonexistent in this case and improbable in other cases. The Board's position would abrogate § 154(b) as patent owners file unwarranted terminal disclaimers as a hedge against their continuations

receiving adjustments that would invalidate other family members. Once terminally disclaimed, the patent owner receives no recompense for government delay that eats into the owner's statutorily granted patent term. *See* 35 U.S.C. § 154(b)(2)(B). Such a result is inequitable and does not achieve the goals of Congress ***or*** double patenting.

IV. THERE IS NO SUBSTANTIAL NEW QUESTION OF PATENTABILITY HERE BECAUSE THE EXAMINER CONSIDERED DOUBLE PATENTING DURING PROSECUTION AND KNEW OF THE ADJUSTMENTS

The Board fundamentally erred in finding a substantial new question of patentability exists in this case, because (1) the same Examiner examined all of the Challenged Patents and the alleged double patenting reference, the '036 Patent, determined that double patenting did not apply; and (2) Examiner Rao knew of the PTAs and their length from the Notices of Allowance under the ***then-current*** statutory scheme, such that the Board was simply wrong that the information was unavailable until issuance.[6] *See generally* Appx21-22, Appx46, Appx70-71, Appx94-95. Examiner Rao did, in fact, have the PTAs before him during prosecution, because they were included with the Notices of Allowance. The

[6] Only for the '742 Patent, the Board claimed that the PTA constituted a new question of patentability and that Examiner Rao did not consider double patenting. Appx21-22. In the '369, '626, and '621 Patent Decisions, the Board only claimed that Examiner Rao did not consider double patenting. Appx46, Appx70-71, Appx94-95. As demonstrated below, both assertions of the Board are incorrect.

version of 37 C.F.R. § 1.705 that was in force during prosecution of the Challenged Patents required that notices of allowance identify the PTAs. Appx516, Appx1000, Appx6853, Appx9717 (adjustment decisions with Notices of Allowance for the Challenged Patents). Thus, the Board's claim that "at the time of a notice of allowance, an examiner does not necessarily know whether the resulting patent will receive any PTA or if so how much" is simply wrong. Appx22.

Examiner Rao's knowledge of the Patents at Issue and the actions he took during prosecution to evaluate patentability demonstrates that he considered potential double patenting issues. First, the Challenged Patents and the '036 Patent belong to the same patent family, have the same inventors, and have the same assignee. Appx132, Appx163, Appx189, Appx216, Appx6387. Second, the same examiner, Examiner Rao, prosecuted all the relevant applications during the same timeframe. *Id.* Third, he was not shy about issuing a double patenting rejection when warranted. He, in fact, issued one during prosecution of the related '255 Patent Application, which is the parent to the '369 and '626 Patents and grandparent to the '742 and '621 Patents. Appx3259-3262 (Office Action based on double patenting for '255 Patent).

Fourth, Examiner Rao conducted interference searches that would have identified any same or similar claims in conflict with the claims of the applications

of the Challenged Patents. *See, e.g.*, Appx524-525 (interference search notes from the '742 Patent file history); Appx1017 (interference search notes from the '369 Patent file history); Appx6880 (interference search notes from the '626 Patent file history); Appx9724 (interference search notes from the '621 Patent file history). Mr. Spar, an expert on Patent Office examination practices and procedures, considered these searches and the other indicia of Examiner Rao's diligence during prosecution demonstrate that the examiner did in fact consider double patenting, and found nothing of concern. Appx2441-2443, Appx8110-8113, Appx10912-10915. The Board simply never addressed this evidence.

The fact that Examiner Rao examined the applications in parallel highlights that he was keenly aware of and considered the reference patents. During the prosecution of the '742 and '621 Patent Applications, Examiner Rao explicitly considered each application's respective parent, the '369 and '626 Patents. *See, e.g.*, Appx524, Appx9721, Appx9724. He initialed next to the parent of the '621 Patent on an IDS, confirming he expressly considered it. Appx9721 (initialed IDS from the '621 Patent file history, listing the parent '626 Patent); MPEP § 609 (examiner initials indicate information was considered). He identified the parent applications of the '742 Patent and '621 Patent as search terms in the descriptions of his search strategies for each prosecution, again confirming he considered those parent applications. Appx524 (search terms from the '742 Patent file history,

identifying the parent '369 Patent by its application number), Appx9724 (search terms from the '621 Patent file history, identifying the parent '626 Patent by its application number). Indeed, the parent-child relationship ***required*** Examiner Rao to consider the child applications in light of the parent patents—and he annotated the files properly to show that he did. *See* MPEP § 609.02 ("The examiner will consider information which has been considered by the Office in a parent application . . . ."). Yet here, the Patent Office uses the parent '369 and '626 Patents to invalidate their children, the '742 and '621 Patents, even though the Examiner determined they did not impact validity.

Additionally, there is ample undisputed evidence in the relevant prosecution histories of the Challenged Patents that Examiner Rao was well-aware of the other patents in the family and their interrelatedness because he considered various other related patents during prosecution—not just the parent applications. *See, e.g.*, Appx9721 (initialed IDS from the '621 Patent file history, listing the '626 and '036 Patents); Appx531 (initialed IDS from the '742 Patent file history, listing the '626 and '036 Patents); Appx9724 (search terms from the '621 Patent file history, identifying the '626 and '742 Patents by their application numbers); Appx524 (search terms from the '742 Patent file history, identifying the '369 and '621 Patents by their application numbers).

He also considered related patents earlier in the priority chain during the prosecution of the '742, '369, and '621 Patents. *See, e.g.*, Appx520 (initialed IDS from the '742 Patent file history, listing the '901 Patent); Appx9731-9732 (initialed IDS from the '621 Patent file history, listing the '901 Patent); Appx9724 (search terms from the '621 Patent file history, identifying the '839 Patent by its application number); Appx992 (initialed IDS from the '369 Patent file history, listing the '901 Patent).

Further, Examiner Rao considered the applicability of some of the same alleged prior art across multiple prosecutions of Cellect's related patents. *See, e.g.*, Appx437-440, Appx947-953, Appx6785-6788, Appx9664-9667 (Office Actions asserting Jacobsen *et al.* as a prior art reference in the '742, '369, '626, and '621 Patents' file histories). His search strategy for the '742 and '621 Patents also included an inventor name search, which would have returned the Challenged Patents' parent patents as references given their shared inventors, as well as other Cellect patent applications. Appx524 (search terms from the '742 Patent file history), Appx9724 (search terms from the '621 Patent file history). There is no question that the examiner was well-aware of Cellect's patent family.

There is no substantial new question of patentability where "the same question of patentability has already been . . . decided in an earlier concluded examination or review of the patent by the Office." MPEP § 2242 ("earlier

concluded examination" includes "the original examination of the application which matured into the patent"). The Board's Decisions ignore the evidence that Examiner Rao considered any double patenting issue with respect to the Patents at Issue here, and instead boil down to questioning Examiner Rao's judgment. *See* Appx21, Appx46, Appx71, Appx95. Merely questioning judgment is insufficient to raise a substantial new question. *See* 35 U.S.C. § 303(a) (requiring "substantial new question"); MPEP § 2242; *see also* H.R. Rep. No. 107-120 (2001) at 3 (Congress intended to limit substantial new questions under § 303(a) so that "[t]he issue raised must be more than just questioning the judgment of the examiner").

Further, the Board erred in its Decision for the '742 Patent by applying the wrong version of 37 C.F.R. § 1.705, which explains when a PTA will be communicated to a patent owner. *Compare* 37 C.F.R. § 1.705 (pre-2013-04-01) ("[t]he notice of ***allowance*** will include . . . any patent term adjustment") *with* 37 C.F.R. § 1.705 (current) ("[t]he ***patent*** will include . . . any patent term adjustment") (emphases added). The Board relied on the current version of 37 C.F.R. § 1.705, as explained in the current MPEP § 2733, to conclude that Examiner Rao did not know about the existence or length of the term adjustments during prosecution because "a patent term adjustment calculation is performed after the notice of allowance" and is "indicated on the patent." Appx21-22 (quoting MPEP § 2733, which explains requirements of 37 C.F.R. § 1.705).

To the contrary, Examiner Rao did know about the adjustment during prosecution. For patents issued prior to January 14, 2013, which includes the '742 Patent (as well as the other Challenged Patents), the Patent Office provided an adjustment determination with the written notice of allowance. 37 C.F.R. § 1.705; *see also* MPEP § 2733 (discussing revisions to 37 C.F.R. § 1.705). Patents issuing after January 14, 2013, receive an adjustment determination upon issuance, which did not apply to the Challenged Patents. Thus, the Board erroneously cast Cellect's term adjustments as providing "new light" on patentability for the '742 Patent. Appx516, Appx1000, Appx6853, Appx9717 (adjustment determinations in Notices of Allowance for the '742, '369, '626, and '621 Patents). The patents in Cellect's patent family all issued between 2002 and 2006, well before the change. Appx132, Appx163, Appx189, Appx216. Since Examiner Rao knew of the term adjustments and their length during prosecution of the Challenged Patents, the Board's cursory conclusion that the adjustments in this case cast "new light" indicating a substantial new question is wrong.

The Board's arguments on substantial new question highlight the arbitrariness of the precedent it seeks to establish. In the Board's view, a substantial new question arises when challenged Patent A receives a longer term adjustment than Patent B, which receives only a short adjustment. The Board claims the adjustment creates a substantial new question if that adjustment causes

challenged Patent A to expire later than Patent B, even though challenged Patent A would otherwise have expired before Patent B (making Patent B unavailable as a reference). *See, e.g.*, Appx22 ('742 Decision). But under this scheme, if Patent A received just a little less adjustment—even a matter of one day less—Patent B would remain later-expiring and inappropriate as a reference. This shifting sands approach, in which the issuance of each related patent could affect even already-issued patents solely due to an adjustment, sows confusion and uncertainty in continuation practice. Such an arbitrary result cannot have been the Congressional intent for term adjustments nor the judicial intent for addressing double patenting concerns.

Thus, the Board improperly concluded that Examiner Rao did not consider double patenting and did not know about the adjustments during prosecution, compelling reversal.

V. EVEN IF THIS COURT PERMITS TERM ADJUSTMENTS TO RETROACTIVELY CREATE DOUBLE PATENTING ISSUES, ONLY THE ADJUSTMENT SHOULD BE CONSIDERED FOR INVALIDATION

If the judicially created doctrine of double patenting is expanded to include patents whose expiration dates differ solely because of congressionally mandated term adjustments, this Court should at least draw the line to avoid invalidating an entire patent for circumstances outside a patent owner's control. Patent owners facing double patenting objections after issuance should have the opportunity to

decline the adjustment so they can avoid invalidation of an otherwise valid patent. Indeed, this Court appeared to signal in *Novartis* that any double patenting concern would affect the validity of the ***extension***, not the patent, contrary to the Board's position in this case. *See* 909 F.3d at 1369 ("double patenting does not invalidate an otherwise validly obtained PTE").

The facts of this case highlight why invalidation of the entire patent is unjust and illogical. Cellect's patents share a priority claim and would have expired on the same date, but for Patent Office delays affecting four of the applications ranging from 45 to 759 days. The Board concedes that, at least as to the '369 Patent, there can be no double patenting allegation absent staggered expiration dates. *Compare* Appx26-49 ('369 Decision) *generally with* Appx18 ('742 Decision) (the '369 Decision is silent whereas the '742 Decision erroneously alleged double patenting was proper notwithstanding the adjusted expiration dates). Cellect and other patent owners would sooner forego the adjustment and accept the loss of term due to administrative delay, than watch a validly obtained patent—the result of significant investment—turn to ashes in their hands, struck by the lightning of an unfortunate term adjustment. Allowing the patent owner to forego the adjustment is still an inequitable result and inconsistent with Congressional intent, but it is at least less inequitable than the Board's drastic approach.

VI. THE BOARD'S REMAINING INVALIDITY ALLEGATIONS DEPEND ON DOUBLE PATENTING AND THUS COLLAPSE

Because the Board's remaining grounds for invalidity depended on a combination of alleged double patenting with 35 U.S.C. § 103 references, there again can be no finding of invalidity for the same reasons explained above. Specifically, the Board applied the Harris, Tran, and Nguyen references in combination with the alleged double patenting against the '742 Patent, '369 Patent, and '626 Patent, respectively, and summarily concluded obviousness. Appx24, Appx49, Appx73 (Board's Decisions). The Board offered no explanation as to how the additional § 103 references render a Challenged Patent obvious in combination with a double patenting reference, much less how they could invalidate by themselves. Since these patents are not obvious due to alleged double patenting, however, the unexplained addition of a § 103 reference cannot shore up the Board's deficient analysis. Thus, the Board's additional invalidity grounds must fail because the '742 Patent, '369 Patent, and '626 Patent are not subject to the double patenting doctrine and nothing in the record supports that the alleged § 103 references alone invalidate.

CONCLUSION

The judgment should be reversed because double patenting does not apply to the Challenged Patents.

Respectfully submitted,

Dated: May 16, 2022

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ADDENDUM – TABLE OF CONTENTS

UNITED STATES PATENT AND TRADEMARK OFFICE

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte Cellect LLC
Patent Owner and Appellant

Appeal 2021-005303
Reexamination Control 90/014,453
Patent 6,982,742 B2
Technology Center 3900

Before JAMESON LEE, ALLEN R. MacDONALD, and MICHAEL J. ENGLE, *Administrative Patent Judges*.

ENGLE, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. §§ 134(b) and 306, Appellant[1] appeals from the rejection of claims 22, 42, 58, and 66 of U.S. Patent No. 6,982,742 B2 ("the '742 patent" or "challenged patent") in this *ex parte* reexamination. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

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[1] Appellant states that the real party in interest is "Cellect LLC, a wholly owned subsidiary of Micro Imaging Solutions LLC." Appeal Br. 2.

TECHNOLOGY

The application relates to "solid state image sensors which are configured to be of a minimum size and used within miniature computer systems known as palm top computers, personal digital assistants (PDA), or handheld computers/organizers." '742 patent, 1:21–26.

RELATED MATTERS

The challenged patent and its patent family have been involved in a number of proceedings before federal district courts and the USPTO. Appeal Br. 2–3 (listing 1 district court case, 20 *inter partes* review petitions, and 5 *ex parte* reexamination requests). Four of the reexaminations involve substantially similar issues on double patenting. *See* Appeal Nos. 2021-005046; 2021-005258; 2021-005302; 2021-005303.

For the challenged patent, three petitions for *inter partes* review were denied institution because "the scope of challenged claims 22, 42, 58, and 66 is uncertain." IPR2020-00559, Paper 14, at 17 (July 21, 2020); IPR2020-00560, Paper 14, at 16 (July 21, 2020); IPR2020-00561, Paper 14, at 17 (July 21, 2020). As it was not raised in the present proceeding, we do not address indefiniteness here.

REJECTIONS

Claims 22, 42, 58, and 66 of the '742 patent are rejected for non-statutory double patenting over claims 1, 17, 28, 30, 49, 58, and 61 of U.S. Patent No. 6,424,369 ("the '369 patent" or "reference patent"). Final Act. 13–21.

Claims 22, 42, 58, and 66 of the '742 patent are rejected for non-statutory double patenting over claims 1, 17, 28, 30, 49, 58, and 61 of the '369 patent in view of Harris (US 6,009,336). Final Act. 21.

ISSUE

Did the Examiner err in applying an obviousness-type double patenting rejection to two related patents that (1) claim the same priority date, (2) have different patent term adjustments, and (3) are expired?

ANALYSIS

Overview

The challenged patent (the '742 patent) is the child of the reference patent (the '369 patent). The challenged patent issued after the reference patent, but both claim priority to the same application (filed Oct. 6, 1997) so they normally would expire at the same time (Oct. 6, 2017).[2] 35 U.S.C. § 154(a)(2). However, due to various delays by the USPTO during prosecution, both were granted a patent term adjustment ("PTA") under 35 U.S.C. § 154(b), with the challenged patent receiving significantly more PTA than the reference patent (726 days vs. 45 days). Therefore, the reference patent expired *before* the challenged patent. Both patents are now expired, but the statute of limitations for past damages has not yet passed. 35 U.S.C. § 286.

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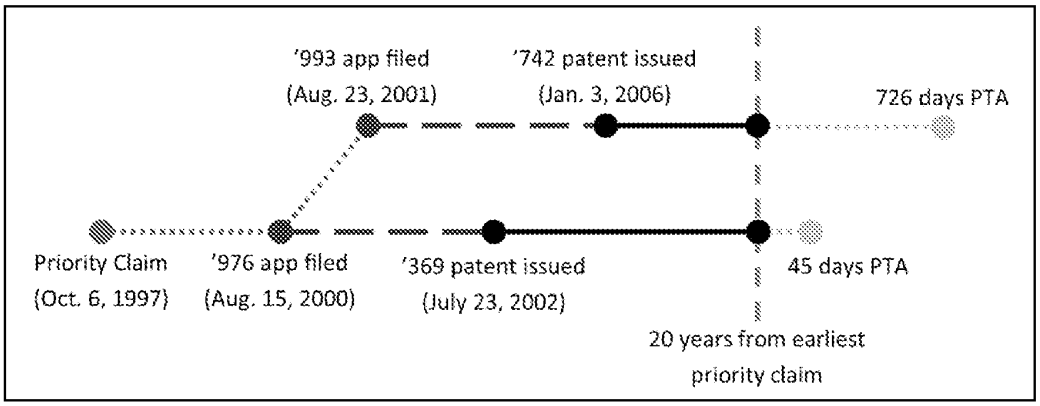
[2] We agree with the Examiner that whether the claims are actually entitled to the claimed date is not relevant to a double patenting analysis. Ans. 4, 9; Appeal Br. 21–24. By statute, expiration is based on a priority date "if the application *contains a specific reference to an earlier filed application*," regardless whether any claim is actually entitled to that priority date. 35 U.S.C. § 154(a)(2) (emphasis added).

The timeline below shows the relevant dates for the two patents, including priority, filing, issuance, expiration, and PTA, with the challenged patent on top and its parent (the reference patent) below:



Timeline for expiration of '742 patent (top) & '369 patent (bottom)

In this reexamination, the examiners invoked the doctrine of obviousness-type double patenting to reject the claims of the challenged patent as obvious variants of claims in the reference patent. Final Act. 13–21. Appellant does not dispute that the claims of the reference patent would have rendered obvious the claims of the challenged patent. Instead, Appellant argues the reference patent cannot be used for double patenting because (1) a judicially-created doctrine cannot take away statutorily guaranteed time, especially in light of the Federal Circuit's treatment of patent term extensions ("PTE") under 35 U.S.C. § 156, (2) the result would be inequitable given the facts here, and (3) no substantial new question of patentability has been raised because the examiner should have considered double patenting in the original prosecution. *See* Appeal Br. 4–21.

We are not persuaded by Appellant's arguments. First, unlike a PTE under § 156, the statute for a PTA (§ 154) states that any terminal disclaimer should be applied *after* any PTA. Because the primary purpose of a terminal

disclaimer is to overcome double patenting, the same rule should apply to double patenting. Moreover, even if double patenting was based on the expiration date *before* applying any PTA (akin to a PTE), double patenting still would be appropriate here because two patents that are obvious variants and expire on the same day still need a terminal disclaimer to enforce common ownership. Second, the result here is not inequitable because the Federal Circuit has said the existence of any extra term of a second patent is itself what is inequitable, and Appellant still enjoyed the entire term of the earliest patent. Third, double patenting is a substantial new question because, regardless of what should have happened in the original prosecution, there is insufficient evidence that the original examiner actually considered double patenting.

Standard of Review

The PTO is "authorized during reexamination to consider the question of double patenting." *In re Lonardo*, 119 F.3d 960, 966 (Fed. Cir. 1997); *see also* MPEP § 2258(I)(D). "As with statutory obviousness under 35 U.S.C. § 103, obviousness-type double patenting is an issue of law premised on underlying factual inquiries." *Eli Lilly & Co. v. Teva Parenteral Meds., Inc.*, 689 F.3d 1368, 1376 (Fed. Cir. 2012).

Legal Background
on Obviousness-Type Double Patenting, Terminal Disclaimers, PTA, & PTE

Obviousness-type double patenting is a "judicially created" doctrine that "prohibits an inventor from obtaining a second patent for claims that are not patentably distinct from the claims of the first patent." *Lonardo*, 119 F.3d at 965. "There are two justifications for obviousness-type double

patenting": (1) "to prevent unjustified timewise extension of the right to exclude granted by a patent no matter how the extension is brought about" and (2) "to prevent multiple infringement suits by different assignees asserting essentially the same patented invention." *In re Hubbell*, 709 F.3d 1140, 1145 (Fed. Cir. 2013) (quotation omitted). For example, if an inventor receives a second patent with claims that are merely obvious variants of a first patent, double patenting helps prevent the patentee from (1) suing on the second patent after the first has already expired (i.e., improper time-wise extension) or (2) selling the two patents to different entities only to have both entities separately sue an alleged infringer on two obvious variants of each other (i.e., improper harassment by multiple assignees).

A patentee or applicant often can overcome double patenting by filing a terminal disclaimer. *Boehringer Ingelheim Int'l GmbH v. Barr Labs., Inc.*, 592 F.3d 1340, 1346 (Fed. Cir. 2010). Terminal disclaimers are expressly permitted by statute to "disclaim or dedicate to the public . . . any terminal part of the term" of a patent. 35 U.S.C. § 253(b). The USPTO has provided regulations on what a terminal disclaimer must contain to be effective. *E.g.*, 37 C.F.R. § 1.321. A terminal disclaimer solves the two concerns of double patenting by (1) making the *later* patent expire with the *earlier* patent and (2) rendering the second patent unenforceable if it is not commonly owned with the first patent. *E.g.*, 37 C.F.R. § 1.321(b)(2), (c)(3), (d)(3); MPEP §§ 804.02(VI), 1490(VI)(A), (IX). However, "a terminal disclaimer filed after the expiration of the earlier patent over which claims have been found obvious cannot cure obviousness-type double patenting." *Boehringer*, 592 F.3d at 1347–48. Thus, a terminal disclaimer cannot cure any double patenting rejection against the expired patents here. Appeal Br. 19.

For two issued patents, double patenting and the need for a terminal disclaimer generally only apply to the *later* patent.[3] *See Eli Lilly & Co. v. Barr Labs., Inc.*, 251 F.3d 955, 968 & n.5 (Fed. Cir. 2001) ("A *later* claim that is not patentably distinct from an earlier claim in a commonly owned patent is invalid for obvious-type double patenting."; "A patent owner cannot avoid double patenting by disclaiming the *earlier* patent." (emphases added)). The question then is how to determine which patent is "later." The answer depends on whether the patents issued from applications filed on or after June 8, 1995. This date is six months after enactment of the Uruguay Round Agreements Act ("URAA"), which changed the term of a patent from (A) 17 years after issue to (B) 20 years from the earliest filing date of any non-provisional U.S. application to which that patent claims priority. 35 U.S.C. § 154.

For two post-URAA patents, the "later" patent generally is determined by looking at the *expiration* date. *Novartis Pharms. Corp. v. Breckenridge Pharm. Inc.*, 909 F.3d 1355, 1362–63, 1366 (Fed. Cir. 2018). For two pre-URAA patents or certain scenarios involving one patent on each side of the URAA date, the "later" patent is instead determined by looking at the *issue* date. *Id.* at 1362 ("Traditionally, courts looked at the issuance dates of the respective patents, because, under the law pre-URAA, the expiration date of the patent was inextricably intertwined with the issuance date, and used the earlier-issued patent to limit the patent term(s) of the later issued patent(s)."). Prior to the URAA, a patent expired 17 years after issuance, so

[3] For two co-pending applications, a provisional double patenting rejection against both applications may be appropriate if it is not yet known which will result in the later patent. *See* MPEP § 804(I)(1).

"looking to patent issue dates had previously served as a reliable stand-in for the date that really mattered—patent expiration." *Gilead Scis., Inc. v. Natco Pharma Ltd.*, 753 F.3d 1208, 1215 (Fed. Cir. 2014). Finally, if two post-URAA patents expire on the same day or two pre-URAA patents have the same issue date, then the patent with the higher patent number may be invalid for double patenting.[4] *See Underwood v. Gerber*, 149 U.S. 224 (1893) (affirming Patent No. 348,073 was void over the same inventors' Patent No. 348,072 when both patents had the same filing date, issue date, and expiration date).

A complication arises, however, in that Congress also provided two ways to potentially prolong the term of a patent. A patent term adjustment ("PTA") under § 154(b) may adjust the term based on certain delays by the USPTO during prosecution, and a patent term extension ("PTE") under § 156 may extend the term based on certain regulatory delays, such as the FDA reviewing a new drug. 35 U.S.C. §§ 154(b), 156. The question before us now is how a PTA under § 154 should factor into the double patenting analysis, such as whether double patenting should be based on the expiration date *before* a PTA or *after*. The Federal Circuit already addressed similar questions for a PTE, yet it did so by contrasting the statutes for PTE (§ 156) versus PTA (§ 154). We discuss these cases below.

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[4] As the patents here issued on different dates, we need not resolve whether an analysis for patents issued on the same day should first look to priority date or filing date rather than patent number (e.g., two pre-URAA patents with the same issue date but the patent with the higher patent number has a significantly earlier filing date and priority date).

PTE & Terminal Disclaimers
(Merck v. Hi-Tech)

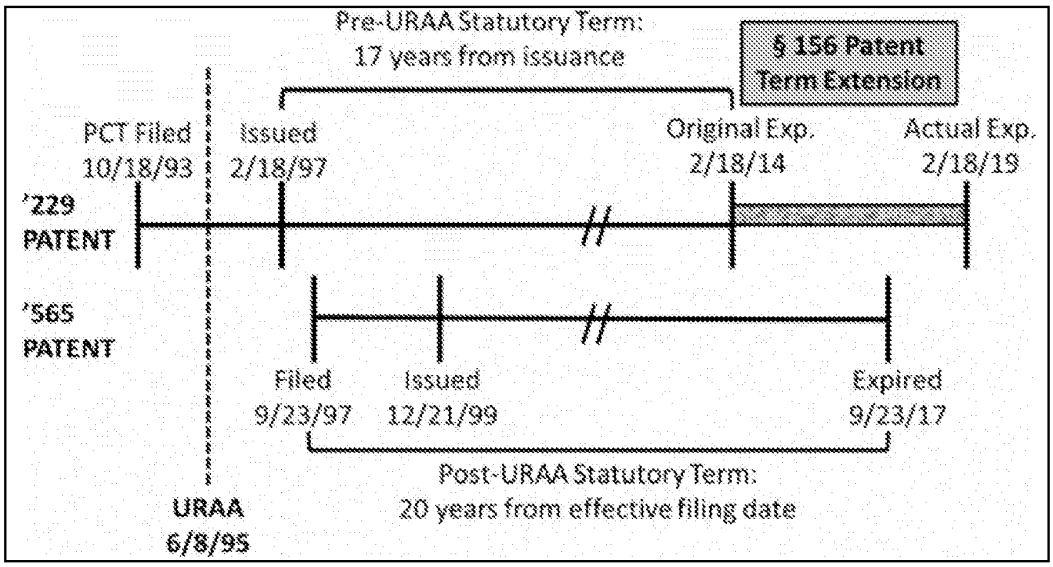
For a PTE under § 156, the starting point is *Merck & Co. v. Hi-Tech Pharmacal Co.*, 482 F.3d 1317 (Fed. Cir. 2007). In that case, the patent owner had already filed a terminal disclaimer to overcome an obviousness-type double patenting rejection. 482 F.3d at 1318–19. Later, the patent was awarded a PTE under § 156. *Id.* at 1319. The question before the court was whether a PTE under § 156 could be applied to a patent subject to a terminal disclaimer. *Id.* at 1324. The court held "a patent term extension under § 156 is not foreclosed by a terminal disclaimer." *Id.* at 1322. In particular, "[t]he computation of a Hatch–Waxman patent term extension is from the expiration date resulting from the terminal disclaimer and not from the date the patent would have expired in the absence of the terminal disclaimer." *Id.* at 1322–23. Put another way, a PTE under § 156 is applied *after* any terminal disclaimer.

The Federal Circuit reached this conclusion by contrasting PTE with PTA. For a PTA, "§ 154(b)(2)(B) expressly excludes patents in which a terminal disclaimer was filed from the benefit of a term adjustment for PTO delays." *Merck v. Hi-Tech*, 482 F.3d at 1322. Specifically, the statute states that "[n]o patent the term of which has been disclaimed beyond a specified date may be adjusted under this section beyond the expiration date specified in the disclaimer." 35 U.S.C. § 154(b)(2)(B). The Federal Circuit explained that "[t]here is no similar provision that excludes patents in which a terminal disclaimer was filed from the benefits of Hatch-Waxman extensions" under § 156. *Merck v. Hi-Tech*, 482 F.3d at 1322. Thus, a terminal disclaimer is applied *before* a PTE *because* PTE is different than PTA.

PTE & Double Patenting
(Novartis v. Ezra)

The next question was how a PTE applied to double patenting in the absence of a terminal disclaimer. As noted above, a terminal disclaimer generally is filed to overcome obviousness-type double patenting. *In re Van Ornum*, 686 F.2d 937, 948 (CCPA 1982); 37 C.F.R. § 1.321(c), (d); MPEP § 1490(II). Given this relationship between double patenting and terminal disclaimers and given the holding in *Merck v. Hi-Tech* that a terminal disclaimer applies *before* a PTE, the Federal Circuit not surprisingly held "as a logical extension of our holding in *Merck & Co. v. Hi-Tech*" that double patenting also should be considered *before* a PTE. *Novartis AG v. Ezra Ventures LLC*, 909 F.3d 1367, 1373–74 (Fed. Cir. 2018). Thus, "if a patent, under its original expiration date without a PTE, should have been (but was not) terminally disclaimed because of obviousness-type double patenting, then this court's obviousness-type double patenting case law would apply, and the patent could be invalidated." *Id.* at 1374. "However, if a patent, under its pre-PTE expiration date, is valid under all other provisions of law, then it is entitled to the full term of its PTE." *Id.*

A timeline for the patents in *Novartis v. Ezra* is reproduced below:



Novartis v. Ezra, 909 F.3d at 1370. As shown in the timeline above, the challenged patent (the '229 patent) had an *earlier* filing date, issue date, and pre-PTE expiration date than the reference patent (the '565 patent). Because the challenged patent was the *earlier* patent (at least pre-PTE), the challenged patent was not invalid for double patenting. *Id.* at 1373–75.

PTA & Double Patenting

The question now before us is how a PTA affects double patenting. Appellant relies on one broadly worded sentence in *Novartis v. Ezra* to argue that "a judge-made doctrine" (i.e., obviousness-type double patenting) cannot "cut off a statutorily-authorized time extension." Appeal Br. 11 (quoting *Novartis v. Ezra*, 909 F.3d at 1375). Although the holding in *Novartis v. Ezra* was about a PTE under § 156, Appellant extends that argument to suggest that any PTA under § 154 also is a "statutory grant of additional term" that "cannot be deemed improper." *Id.* at 12.

Appellant's argument is not persuasive because it ignores the plain text of § 154 and the actual holding in *Novartis v. Ezra*.

First, contrary to Appellant's assertions, the decision in *Novartis v. Ezra* reaffirms that a double patenting analysis *should* be done even if a patent has a PTE. The real question was whether double patenting should be considered *before* or *after* a PTE, with the court ultimately deciding double patenting should be considered *before* a PTE. *Novartis v. Ezra*, 909 F.3d at 1374 ("if a patent, under its original expiration date without a PTE, should have been (but was not) terminally disclaimed because of obviousness-type double patenting, then this court's obviousness-type double patenting case law would apply, and the patent could be invalidated"). So here, we must do a double patenting analysis and the question is whether double patenting should be considered with the expiration dates *before* or *after* a PTA.

Second, the outcome for a PTE under § 156 in *Merck v. Hi-Tech* was based on the difference between § 156 and § 154. In particular, "§ 154(b)(2)(B) expressly excludes patents in which a terminal disclaimer was filed from the benefit of a term adjustment for PTO delays," but there is an "absence of any such prohibition regarding Hatch–Waxman extensions" under § 156. *Merck v. Hi-Tech*, 482 F.3d at 1322. That reasoning in *Merck v. Hi-Tech* was important enough that when summarizing the prior case, *Novartis v. Ezra* repeated the prior case's "contrast between § 156 for PTE with the language of § 154 for patent term adjustments." *Novartis v. Ezra*, 909 F.3d at 1373–74. Thus, the rule in *Merck v. Hi-Tech* and *Novartis v. Ezra* for when to apply a PTE does not apply to a PTA because those decisions were premised on the contrast between PTE and PTA.

Third, the statutory language in § 154 is clear that any terminal disclaimer should be applied *after* any PTA (i.e., a PTA cannot adjust a term beyond the expiration date in any disclaimer). 35 U.S.C. § 154(b)(2)(B) ("No patent the term of which has been disclaimed beyond a specified date may be adjusted under this section beyond the expiration date specified in the disclaimer."). Although Appellant asserts that the statute says the term "shall" be extended (Reply Br. 8), Appellant omits that all of those sentences are prefaced with the phrase "Subject to the limitations under paragraph (2)," which includes the limitations due to terminal disclaimers. *Id.* § 154(b)(1)(A), (B), (C). Thus, as recognized by *Merck v. Hi-Tech* and *Novartis v. Ezra*, the statute itself is clear that unlike a PTE under § 156, a PTA under § 154 shall *not* extend the term of a patent past the date of any terminal disclaimer.

Fourth, given that terminal disclaimers arise almost exclusively to overcome obviousness-type double patenting, Congress expressly addressing terminal disclaimers in § 154 is tantamount to addressing obviousness-type double patenting. *See Van Ornum*, 686 F.2d at 948; 37 C.F.R. § 1.321(c), (d); MPEP § 1490(II). Indeed, *Novartis v. Ezra* itself recognized that a rule for terminal disclaimers (from *Merck v. Hi-Tech*) should also apply to obviousness-type double patenting as "a logical extension." 909 F.3d at 1373. The *Novartis v. Ezra* court rejected the argument "that the *Merck* court's rationale only spoke to the impact of a new PTE on preexisting terminal disclaimers," instead finding that the prior "holding on the validity of a PTE for a patent that was terminally disclaimed *in order to overcome an obviousness-type double patenting rejection* is directly relevant to the instant case." *Id.* at 1374 (quotation omitted). Obviousness-type double patenting

and terminal disclaimers are two sides of the same coin: the problem and the solution. Just as *Novartis v. Ezra* found a rule on terminal disclaimers was "directly relevant" to double patenting and therefore applied that rule to double patenting as "a logical extension," so too we hold that the statutory rule for terminal disclaimers in § 154 is directly relevant to double patenting and we apply that same rule to double patenting as a logical extension.

Indeed, in at least one related reexamination, Appellant itself argues that double patenting should be applied to post-PTA dates. *Compare* Appeal 2021-005302, Appeal Br. 7 ("the '369 Patent . . . and '626 Patent . . . have the same expiration date except for statutorily-authorized PTA"), *with id.* at 10 n.1 ("the '626 Patent cannot be used as an obviousness-type double patenting reference because the '626 Patent expired after the '369 Patent").

Finally, the Federal Circuit also previously said that "another crucial purpose of the doctrine" of double patenting was "to prevent an inventor from securing a second, later expiring patent" for "[p]atents . . . filed at the same time" that "have different patent terms due to examination delays at the PTO" under "§ 154(b) (patent term adjustments)." *AbbVie Inc. v. Mathilda & Terence Kennedy Inst. of Rheumatology Tr.*, 764 F.3d 1366, 1373 (Fed. Cir. 2014); *see also In re Fallaux*, 564 F.3d 1313, 1319 (Fed. Cir. 2009) ("In some cases there may still be the possibility of an unjust time-wise extension of a patent arising from patent term adjustment under § 154 or patent term extension under § 156."). That is precisely the scenario we have here where two patents have the same effective filing date but expire at different times due solely to PTAs.

Appellant provides no plausible reason for ignoring the clear statutory text and the contrast between § 154 and § 156 that formed the basis of *Merck*

v. Hi-Tech and *Novartis v. Ezra*. Nor has Appellant provided any reason for applying the *post*-PTA date for terminal disclaimers yet the *pre*-PTA date for double patenting.[5] We therefore hold that both obviousness-type double patenting and terminal disclaimers should be considered *after* any PTA.[6]

The District Court Decision in Mitsubishi Is Not Persuasive

Appellant also cites a district court decision in *Mitsubishi Tanabe Pharma Corp. v. Sandoz, Inc.*, No. 3:17-cv-05319, __ F. Supp. 3d __, 2021 WL 1845499, at *27–30 (D.N.J. Mar. 22, 2021). Appeal Br. 13–17. We do not find Appellant's citation to *Mitsubishi* persuasive. *See also* Ans. 8.

First, an earlier district court decision in the Western District of Michigan came out the opposite way from *Mitsubishi*. *Magna Elecs., Inc. v. TRW Automotive Holdings Corp.*, No. 12-cv-654, 2015 WL 11430786 (W.D. Mich. Dec. 10, 2015). Although the *Magna Electronics* case appears to have settled prior to any appeal, we understand that the decision in *Mitsubishi* is currently on appeal to the Federal Circuit (No. 21-1876; filed Apr. 23, 2021).

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[5] Applying different dates for double patenting versus terminal disclaimers also creates inconsistent results. For example, suppose the pre-PTA expiration date of Patent A is 1 day after Patent B. Therefore, Patent B could be used as a double patenting reference (pre-PTA) against Patent A, and a terminal disclaimer (post-PTA) would wipe out *all* PTA on Patent A. However, Patent A could *not* be used as a double patenting reference (pre-PTA) against Patent B, so Patent B could have an unlimited amount of PTA, even long after the expiration of Patent A.

[6] 35 U.S.C. § 154(b)(3)(A) gives the Director some discretion "establishing procedures for the application for and determination of patent term adjustments." Because we decide the case based on the reasoning above, we need not decide whether that discretion includes the PTA issues here.

Second, the *Mitsubishi* district court never addressed that double patenting applies even to two patents that have the same filing date, the same issue date, and the same expiration date. *Underwood*, 149 U.S. 224. For example, a terminal disclaimer is still needed to ensure that two patents remain commonly owned. *See Sandy MacGregor Co. v. Vaco Grip Co.*, 2 F.2d 655, 657 (6th Cir. 1924) ("in *Underwood v. Gerber* it was thought that the splitting up of one indivisible right into two and subjecting the infringer to suits by two different owners of the right infringed justified applying the defense of double patenting as against two patents issued on the same day"); *Van Ornum*, 686 F.2d at 945 (similarly summarizing *Underwood*).

Third, the district court's entire discussion of the difference between § 154 and § 156 is relegated to a single footnote in which the court does not appear to have understood that a terminal disclaimer is the standard way to cure double patenting, thereby overlooking why the Federal Circuit decided a rule for terminal disclaimers (*Merck v. Hi-Tech*) should also apply to a double patenting analysis (*Novartis v. Ezra*) as a "logical extension." *See Mitsubishi*, 2021 WL 1845499, at *29 n.45.

Fourth, even within the same paragraph, the district court confuses when the challenged patent would have expired relative to the reference patent. *Compare Mitsubishi*, 2021 WL 1845499, at *29 ("absent the PTA granted to the '788 Patent, both the '788 Patent and the '219 Patent would have the same expiration date"), *with id.* ("but for the § 154(b) PTA, the '788 Patent would have expired before the '219 Patent"). So it is not clear whether the district court was even considering the right facts.

Finally, in *Mitsubishi*, the challenged patent issued *before* the reference patent (May 17, 2011 vs. July 17, 2012). 2021 WL 1845499, at

*27–28. That is opposite the present case where the challenged patent issued *after* the reference patent. Thus, even if we treated a PTA like PTE and double patenting were considered *before* a PTA, the outcome here still would be the opposite of *Mitsubishi* because the challenged patent in *Mitsubishi* was the *earlier* patent whereas the challenged patent here is the *later* patent.

For these reasons, we give little weight to the *Mitsubishi* decision.

Double Patenting Here Was Proper Regardless When the PTA Is Applied

As discussed above, we hold that double patenting should be considered *after* any PTA is applied. Here, after applying the PTA, the challenged patent expired after the reference patent (PTA of 726 days vs. 45 days). Appeal Br. 10. Thus, the later-expiring claims of the challenged patent were properly rejected for obviousness-type double patenting over the earlier-expiring claims of the reference patent.

However, even if we treated a PTA like PTE and did a double patenting analysis *before* factoring in any PTA, a double patenting rejection still would be proper here because prior to the PTA, the challenged patent and the reference patent would have expired on the same day (Oct. 6, 2017). *Underwood*, 149 U.S. 224 (affirming a second patent as void when both patents had the same filing date, issue date, and expiration date); *see also* MPEP § 804(I)(B)(1)(b)(ii) ("If both applications are actually filed on the same day, or are entitled to the same earliest effective filing date[,] . . . the provisional nonstatutory double patenting rejection made in each application should be maintained until the rejection is overcome," such as by "filing a terminal disclaimer in the pending application."); Ans. 8 ("ODP is

appropriate to be considered and addressed in reexamination, regardless whether two relevant patents have different expiration[] dates"). Here, the challenged patent is a later-issued patent claiming obvious variants of the earlier-issued reference patent. Even with the same expiration date, double patenting and a terminal disclaimer are still needed to ensure that the later-issued obvious variant retains common ownership with the earlier-issued patent. This is necessary to accomplish double patenting's second goal "to prevent multiple infringement suits by different assignees asserting essentially the same patented invention." *Hubbell*, 709 F.3d at 1145; *see also Sandy MacGregor*, 2 F.2d at 657 ("in *Underwood v. Gerber* it was thought that the splitting up of one indivisible right into two and subjecting the infringer to suits by two different owners of the right infringed justified applying the defense of double patenting as against two patents issued on the same day"); *see also Van Ornum*, 686 F.2d at 945 (similarly summarizing *Underwood*). Appellant never addresses that double patenting applies to patents with the same expiration date.

Appellant does argue that "there has been no harassment by multiple assignees" because the patents have been commonly owned so far and the patents are now expired. Appeal Br. 12. But the statutory time limitation for past damages is "six years prior to the filing of the complaint." 35 U.S.C. § 286. The patents here expired less than six years ago, so the risk still remains for multiple assignees to seek past damages. Indeed, Appellant has already filed one lawsuit after both patents expired. Appeal Br. 2.

Appellant further argues that the patents "will be maintained by the same owner." Appeal Br. 12. The only basis for this assertion is a single paragraph from a declaration of one inventor:

> Because of the exclusive (field-of-use) nature of certain license agreements, MIS/Cellect may not freely assign these patents and they have been, and will continue to be, owned by MIS/Cellect. As the Chief Technology Officer and Co-Founder of Micro Imaging Solutions LLC, I can confirm that MIS/Cellect will not sell off or split apart any portion of the patents that comprise the '742 Patent family to a third-party.

Adair Decl. ¶ 24 (Sept. 28, 2020). But such a declaration is unpersuasive. For example, suppose Appellant went out of business and a bankruptcy court (not Appellant itself) split the patents among various creditors. Even if Appellant's licensees might have a breach-of-contract claim against the new patent owners, a third party sued by the multiple new owners has no way to enforce the inventor's declaration absent double patenting.

There also is no need to wait until *actual* harassment by multiple assignees. *See* Appeal Br. 9 ("this judicially created doctrine requires . . . harassment by multiple assignees"). One goal of double patenting and terminal disclaimers is to preemptively prevent the risk of such harassment:

> Even though both patents are issued to the same patentee or assignee, it (is) possible that ownership of the two will be divided by later transfers and assignments. The possibility of multiple suits against an infringer by assignees of related patents has long been recognized as one of the concerns behind the doctrine of double patenting.

Van Ornum, 686 F.2d at 944 (quoting Chisum on Patents § 9.04(2)(b) (1981)); *see also* Ans. 4.

In sum, the double patenting rejection of the later-issued claims here was proper regardless of whether (A) the PTA is applied before the double patenting analysis (because the challenged patent's post-PTA expiration date is after that of the reference patent) or (B) the PTA is applied after the

double patenting analysis (because despite the pre-PTA expiration dates being the same, the challenged patent is a later-issuing obvious variant still at risk for harassment by multiple assignees).

Substantial New Question

Appellant argues there is no substantial new question of patentability because the examiner in the original prosecution was aware of both applications and "conducted an interference search" for both, so the examiner "would have" made a double patenting rejection "if [the examiner] believed that such a rejection was warranted." Appeal Br. 20–21, 9–10.

We are not persuaded by Appellant's arguments. A substantial new question of patentability does exist here because there is insufficient evidence that double patenting actually was considered during the original prosecution. Regardless of what ideally should have happened during the original prosecution, the reexamination process exists because items sometimes get overlooked or errors are made. *See, e.g.*, *Patlex Corp. v. Mossinghoff*, 758 F.2d 594, 604 (Fed. Cir. 1985) ("The reexamination statute's purpose is to correct errors made by the government . . . and if need be to remove patents that should never have been granted."), *on reh'g*, 771 F.2d 480, 481 (Fed. Cir. 1985) (denying the petition in relevant part).

The Examiner also determines that the PTA itself provided a "new light" for a substantial new question of patentability as the amount of PTA, if any, was not known during prosecution. Ans. 4, 9. In the specific circumstances here, we agree. Generally, a patent term adjustment calculation is performed after the notice of allowance and "the patent term adjustment indicated on the patent is the 'official' notification of the Office's

patent term adjustment determination." MPEP § 2733. Thus, at the time of a notice of allowance, an examiner does not necessarily know whether the resulting patent will receive any PTA or if so how much. Here, the reference patent had already issued in 2002 and been granted 45 days of PTA, whereas the challenged patent did not issue or receive any PTA until 2006. So from 2002 and 2006 (i.e., for most of the prosecution of the application that would result in the challenged patent), the reference patent expired *after* the expected expiration date for the challenged patent (which did not yet have any PTA), not *before* it.

Equity

Appellant argues that "an equitable doctrine should not be applied in a manner that would be inequitable" given that "filing a terminal disclaimer now is not possible as the patents are expired" and "the record is completely devoid" of any "gamesmanship" or "unjustified or improper timewise extension." Appeal Br. 19–20 (quotation omitted).

However, the Federal Circuit is unambiguous that the inequity here is Appellant's enjoyment of a second patent's term beyond the expiration of the first patent:

> When the claims of a patent are obvious in light of the claims of an earlier commonly owned patent, the patentee can have no right to exclude others from practicing the invention encompassed by the later patent after the date of the expiration of the earlier patent. But when a patentee does not terminally disclaim the later patent before the expiration of the earlier related patent, the later patent purports to remain in force even after the date on which the patentee no longer has any right to exclude others from practicing the claimed subject matter. By permitting the later patent to remain in force beyond the date of the earlier patent's expiration, the patentee wrongly purports to

> inform the public that it is precluded from making, using, selling, offering for sale, or importing the claimed invention during a period after the expiration of the earlier patent.
>
> By failing to terminally disclaim a later patent prior to the expiration of an earlier related patent, a patentee enjoys an unjustified advantage—a purported time extension of the right to exclude from the date of the expiration of the earlier patent. The patentee cannot undo this unjustified timewise extension by retroactively disclaiming the term of the later patent because it has *already* enjoyed rights that it seeks to disclaim.

Boehringer, 592 F.3d at 1347–48 (citations omitted); *see also Lonardo*, 119 F.3d at 965. Appellant also never addresses preserving the public's right to make what is covered by the *earlier* patent after it expired:

> The bar against double patenting was created to preserve that bargained-for right held by the public. *See, e.g., Miller v. Eagle Mfg. Co.*, 151 U.S. 186, 197–98, 202 (1894); . . . *Odiorne v. Amesbury Nail Factory*, 18 F.Cas. 578, 579 (C.C.D.Mass.1819). If an inventor could obtain several sequential patents on the same invention, he could retain for himself the exclusive right to exclude or control the public's right to use the patented invention far beyond the term awarded to him under the patent laws. As Justice Story explained in 1819, "[i]t cannot be" that a patentee can obtain two patents in sequence "substantially for the same invention[] and improvements"; "it would completely destroy the whole consideration derived by the public for the grant of the patent, viz. the right to use the invention at the expiration of the term." *Odiorne*, 18 F.Cas. at 579. Thus, the doctrine of double patenting was primarily designed to prevent such harm by limiting a patentee to one patent term per invention or improvement.

Gilead, 753 F.3d at 1212 (parallel citations omitted).

Even beyond the mere existence of the extra term, Appellant concedes that it actively filed at least one lawsuit on the challenged patent after its

expiration, yet Appellant fails to address whether that lawsuit seeks damages for the extra term of the challenged patent. *See* Appeal Br. 2.

Moreover, invalidating the challenged claims of a *second* patent (or third, fourth, and fifth patents in the case of the numerous related reexaminations here) does not take away Appellant's right to enforce its *first* patent.

Thus, Appellant fails to persuade us that the result here is inequitable.

Conclusion

Appellant argues both double patenting rejections collectively with no separate arguments based on Harris. Accordingly, we sustain the double patenting rejections of claims 22, 42, 58, and 66.

OUTCOME

The following table summarizes the outcome of the rejection:

Claim(s) Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
22, 42, 58, 66		Double patenting: '369 patent	22, 42, 58, 66	
22, 42, 58, 66		Double patenting: '369 patent and Harris	22, 42, 58, 66	
Overall Outcome			22, 42, 58, 66	

TIME TO RESPOND

Requests for extensions of time in this *ex parte* reexamination proceeding are governed by 37 C.F.R. § 1.550(c). *See* 37 C.F.R. § 41.50(f).

AFFIRMED

Appeal 2021-005303
Reexamination Control 90/014,453
Patent 6,982,742 B2

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The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte Cellect LLC
Patent Owner and Appellant

Appeal 2021-005302
Reexamination Control 90/014,454
Patent 6,424,369 B1
Technology Center 3900

Before JAMESON LEE, ALLEN R. MacDONALD, and MICHAEL J. ENGLE, *Administrative Patent Judges*.

ENGLE, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. §§ 134(b) and 306, Appellant[1] appeals from the rejection of claims 1, 17, 19, 21, 22, 27, 49, 55, and 61 of U.S. Patent No. 6,424,369 B1 ("the '369 patent" or "challenged patent") in this *ex parte* reexamination. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

[1] Appellant states that the real party in interest is "Cellect LLC, a wholly owned subsidiary of Micro Imaging Solutions LLC." Appeal Br. 2.

TECHNOLOGY

The application relates to "solid state image sensors which are configured to be of a minimum size and used within miniature computer systems known as palm top computers, personal digital assistants (PDA), or handheld computers/organize." '369 patent, 1:16–21.

RELATED MATTERS

The challenged patent and its patent family have been involved in a number of proceedings before federal district courts and the USPTO. Appeal Br. 2–3 (listing 1 district court case, 20 *inter partes* review petitions, and 5 *ex parte* reexamination requests). Four of the reexaminations involve substantially similar issues on double patenting. *See* Appeal Nos. 2021-005046; 2021-005258; 2021-005302; 2021-005303.

For the challenged patent, three petitions for *inter partes* review were denied institution because "the scope of the claims cannot be determined without undue speculation." IPR2020-00562, Paper 14, at 20 (July 21, 2020); IPR2020-00563, Paper 14, at 19 (July 21, 2020); IPR2020-00564, Paper 14, at 19–20 (July 21, 2020). As it was not raised in the present proceeding, we do not address indefiniteness here.

REJECTIONS

Claims 1, 17, 19, 21, 22, 27, 49, 55, and 61 of the '369 patent are rejected for non-statutory double patenting over claims 1, 17, 19, 21, 22, 27, and 33 of U.S. Patent No. 6,862,036 ("the '036 patent") in view of Tran (US 6,202,060 B1; Mar. 13, 2001). Final Act. 5–39.

Claims 1, 17, 19, 21, 22, 27, 49, 55, and 61 of the '369 patent are rejected for non-statutory double patenting over claims 1, 17, 19, 21, 22, 27,

49, 55, and 61 of U.S. Patent No. 6,452,626 ("the '626 patent") in view of admitted prior art. Final Act. 40–60.

ISSUE

Did the Examiner err in applying an obviousness-type double patenting rejection to two related patents that (1) claim the same priority date, (2) have different patent term adjustments, and (3) are expired?

ANALYSIS

Standard of Review

The PTO is "authorized during reexamination to consider the question of double patenting." *In re Lonardo*, 119 F.3d 960, 966 (Fed. Cir. 1997); *see also* MPEP § 2258(I)(D). "As with statutory obviousness under 35 U.S.C. § 103, obviousness-type double patenting is an issue of law premised on underlying factual inquiries." *Eli Lilly & Co. v. Teva Parenteral Meds., Inc.*, 689 F.3d 1368, 1376 (Fed. Cir. 2012).

Legal Background on Obviousness-Type Double Patenting, Terminal Disclaimers, PTA, & PTE

Obviousness-type double patenting is a "judicially created" doctrine that "prohibits an inventor from obtaining a second patent for claims that are not patentably distinct from the claims of the first patent." *Lonardo*, 119 F.3d at 965. "There are two justifications for obviousness-type double patenting": (1) "to prevent unjustified timewise extension of the right to exclude granted by a patent no matter how the extension is brought about" and (2) "to prevent multiple infringement suits by different assignees asserting essentially the same patented invention." *In re Hubbell*, 709 F.3d 1140, 1145 (Fed. Cir. 2013) (quotation omitted). For example, if an inventor

receives a second patent with claims that are merely obvious variants of a first patent, double patenting helps prevent the patentee from (1) suing on the second patent after the first has already expired (i.e., improper time-wise extension) or (2) selling the two patents to different entities only to have both entities separately sue an alleged infringer on two obvious variants of each other (i.e., improper harassment by multiple assignees).

A patentee or applicant often can overcome double patenting by filing a terminal disclaimer. *Boehringer Ingelheim Int'l GmbH v. Barr Labs., Inc.*, 592 F.3d 1340, 1346 (Fed. Cir. 2010). Terminal disclaimers are expressly permitted by statute to "disclaim or dedicate to the public . . . any terminal part of the term" of a patent. 35 U.S.C. § 253(b). The USPTO has provided regulations on what a terminal disclaimer must contain to be effective. *E.g.*, 37 C.F.R. § 1.321. A terminal disclaimer solves the two concerns of double patenting by (1) making the *later* patent expire with the *earlier* patent and (2) rendering the second patent unenforceable if it is not commonly owned with the first patent. *E.g.*, 37 C.F.R. § 1.321(b)(2), (c)(3), (d)(3); MPEP §§ 804.02(VI), 1490(VI)(A), (IX). However, "a terminal disclaimer filed after the expiration of the earlier patent over which claims have been found obvious cannot cure obviousness-type double patenting." *Boehringer*, 592 F.3d at 1347–48. Thus, a terminal disclaimer cannot cure any double patenting rejection against the expired patents here. Appeal Br. 17–18.

For two issued patents, double patenting and the need for a terminal disclaimer generally only apply to the *later* patent.[2] *See Eli Lilly & Co. v.*

[2] For two co-pending applications, a provisional double patenting rejection against both applications may be appropriate if it is not yet known which will result in the later patent. *See* MPEP § 804(I)(1).

Barr Labs., Inc., 251 F.3d 955, 968 & n.5 (Fed. Cir. 2001) ("A *later* claim that is not patentably distinct from an earlier claim in a commonly owned patent is invalid for obvious-type double patenting."; "A patent owner cannot avoid double patenting by disclaiming the *earlier* patent." (emphases added)). The question then is how to determine which patent is "later." The answer depends on whether the patents issued from applications filed on or after June 8, 1995. This date is six months after enactment of the Uruguay Round Agreements Act ("URAA"), which changed the term of a patent from (A) 17 years after issue to (B) 20 years from the earliest filing date of any non-provisional U.S. application to which that patent claims priority. 35 U.S.C. § 154.

For two post-URAA patents, the "later" patent generally is determined by looking at the *expiration* date. *Novartis Pharms. Corp. v. Breckenridge Pharm. Inc.*, 909 F.3d 1355, 1362–63, 1366 (Fed. Cir. 2018). For two pre-URAA patents or certain scenarios involving one patent on each side of the URAA date, the "later" patent is instead determined by looking at the *issue* date. *Id.* at 1362 ("Traditionally, courts looked at the issuance dates of the respective patents, because, under the law pre-URAA, the expiration date of the patent was inextricably intertwined with the issuance date, and used the earlier-issued patent to limit the patent term(s) of the later issued patent(s)."). Prior to the URAA, a patent expired 17 years after issuance, so "looking to patent issue dates had previously served as a reliable stand-in for the date that really mattered—patent expiration." *Gilead Scis., Inc. v. Natco Pharma Ltd.*, 753 F.3d 1208, 1215 (Fed. Cir. 2014). Finally, if two post-URAA patents expire on the same day or two pre-URAA patents have the same issue date, then the patent with the higher patent number may be

invalid for double patenting.[3] *See Underwood v. Gerber*, 149 U.S. 224 (1893) (affirming Patent No. 348,073 was void over the same inventors' Patent No. 348,072 when both patents had the same filing date, issue date, and expiration date).

A complication arises, however, in that Congress also provided two ways to potentially prolong the term of a patent. A patent term adjustment ("PTA") under § 154(b) may adjust the term based on certain delays by the USPTO during prosecution, and a patent term extension ("PTE") under § 156 may extend the term based on certain regulatory delays, such as the FDA reviewing a new drug. 35 U.S.C. §§ 154(b), 156. The question before us now is how a PTA under § 154 should factor into the double patenting analysis, such as whether double patenting should be based on the expiration date *before* a PTA or *after*. The Federal Circuit already addressed similar questions for a PTE, yet it did so by contrasting the statutes for PTE (§ 156) versus PTA (§ 154). We discuss these cases below.

PTE & Terminal Disclaimers
(Merck v. Hi-Tech)

For a PTE under § 156, the starting point is *Merck & Co. v. Hi-Tech Pharmacal Co.*, 482 F.3d 1317 (Fed. Cir. 2007). In that case, the patent owner had already filed a terminal disclaimer to overcome an obviousness-type double patenting rejection. 482 F.3d at 1318–19. Later, the patent was

[3] As the patents here issued on different dates, we need not resolve whether an analysis for patents issued on the same day should first look to priority date or filing date rather than patent number (e.g., two pre-URAA patents with the same issue date but the patent with the higher patent number has a significantly earlier filing date and priority date).

awarded a PTE under § 156. *Id.* at 1319. The question before the court was whether a PTE under § 156 could be applied to a patent subject to a terminal disclaimer. *Id.* at 1324. The court held "a patent term extension under § 156 is not foreclosed by a terminal disclaimer." *Id.* at 1322. In particular, "[t]he computation of a Hatch–Waxman patent term extension is from the expiration date resulting from the terminal disclaimer and not from the date the patent would have expired in the absence of the terminal disclaimer." *Id.* at 1322–23. Put another way, a PTE under § 156 is applied *after* any terminal disclaimer.

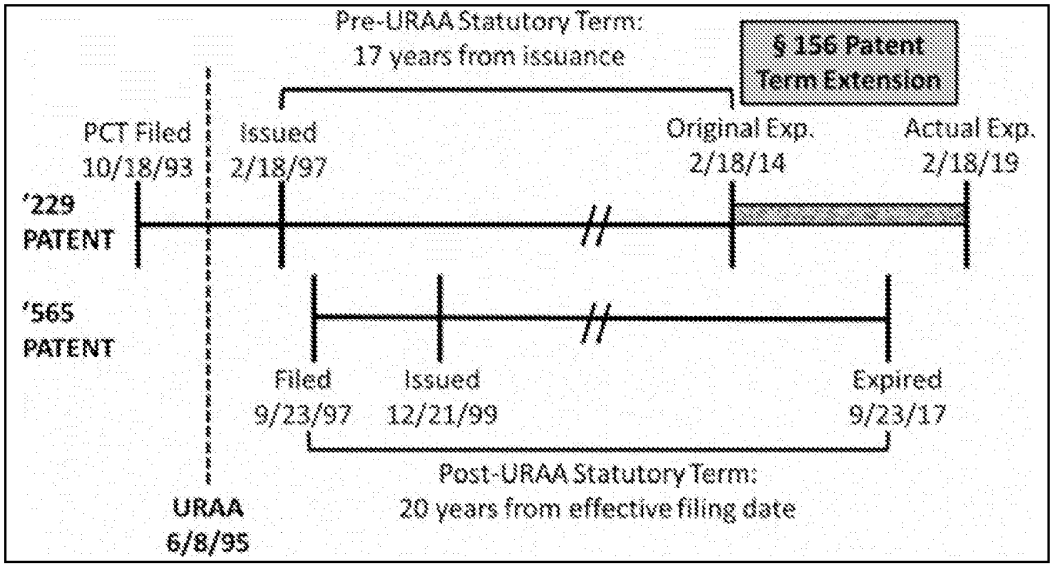
The Federal Circuit reached this conclusion by contrasting PTE with PTA. For a PTA, "§ 154(b)(2)(B) expressly excludes patents in which a terminal disclaimer was filed from the benefit of a term adjustment for PTO delays." *Merck v. Hi-Tech*, 482 F.3d at 1322. Specifically, the statute states that "[n]o patent the term of which has been disclaimed beyond a specified date may be adjusted under this section beyond the expiration date specified in the disclaimer." 35 U.S.C. § 154(b)(2)(B). The Federal Circuit explained that "[t]here is no similar provision that excludes patents in which a terminal disclaimer was filed from the benefits of Hatch-Waxman extensions" under § 156. *Merck v. Hi-Tech*, 482 F.3d at 1322. Thus, a terminal disclaimer is applied *before* a PTE *because* PTE is different than PTA.

PTE & Double Patenting
(Novartis v. Ezra)

The next question was how a PTE applied to double patenting in the absence of a terminal disclaimer. As noted above, a terminal disclaimer generally is filed to overcome obviousness-type double patenting. *In re Van Ornum*, 686 F.2d 937, 948 (CCPA 1982); 37 C.F.R. § 1.321(c), (d); MPEP

§ 1490(II); *see also* Reply Br. 12. Given this relationship between double patenting and terminal disclaimers and given the holding in *Merck v. Hi-Tech* that a terminal disclaimer applies *before* a PTE, the Federal Circuit not surprisingly held "as a logical extension of our holding in *Merck & Co. v. Hi-Tech*" that double patenting also should be considered *before* a PTE. *Novartis AG v. Ezra Ventures LLC*, 909 F.3d 1367, 1373–74 (Fed. Cir. 2018). Thus, "if a patent, under its original expiration date without a PTE, should have been (but was not) terminally disclaimed because of obviousness-type double patenting, then this court's obviousness-type double patenting case law would apply, and the patent could be invalidated." *Id.* at 1374. "However, if a patent, under its pre-PTE expiration date, is valid under all other provisions of law, then it is entitled to the full term of its PTE." *Id.*

A timeline for the patents in *Novartis v. Ezra* is reproduced below:



Novartis v. Ezra, 909 F.3d at 1370. As shown in the timeline above, the challenged patent (the '229 patent) had an *earlier* filing date, issue date, and

pre-PTE expiration date than the reference patent (the '565 patent). Because the challenged patent was the *earlier* patent (at least pre-PTE), the challenged patent was not invalid for double patenting. *Id.* at 1373–75.

PTA & Double Patenting

The question now before us is how a PTA affects double patenting. Appellant relies on one broadly worded sentence in *Novartis v. Ezra* to argue that "a judge-made doctrine" (i.e., obviousness-type double patenting) cannot "cut off a statutorily-authorized time extension." Appeal Br. 10 (quoting *Novartis v. Ezra*, 909 F.3d at 1375). Although the holding in *Novartis v. Ezra* was about a PTE under § 156, Appellant extends that argument to suggest that any PTA under § 154 also is a "statutory grant of additional term" that "cannot be deemed improper." *Id.* at 13.

Appellant's argument is not persuasive because it ignores the plain text of § 154 and the actual holding in *Novartis v. Ezra*.

First, contrary to Appellant's assertions, the decision in *Novartis v. Ezra* reaffirms that a double patenting analysis *should* be done even if a patent has a PTE. The real question was whether double patenting should be considered *before* or *after* a PTE, with the court ultimately deciding double patenting should be considered *before* a PTE. *Novartis v. Ezra*, 909 F.3d at 1374 ("if a patent, under its original expiration date without a PTE, should have been (but was not) terminally disclaimed because of obviousness-type double patenting, then this court's obviousness-type double patenting case law would apply, and the patent could be invalidated"). So here, we must do a double patenting analysis and the question is whether double patenting should be considered with the expiration dates *before* or *after* a PTA.

Second, the outcome for a PTE under § 156 in *Merck v. Hi-Tech* was based on the difference between § 156 and § 154. In particular, "§ 154(b)(2)(B) expressly excludes patents in which a terminal disclaimer was filed from the benefit of a term adjustment for PTO delays," but there is an "absence of any such prohibition regarding Hatch–Waxman extensions" under § 156. *Merck v. Hi-Tech*, 482 F.3d at 1322. That reasoning in *Merck v. Hi-Tech* was important enough that when summarizing the prior case, *Novartis v. Ezra* repeated the prior case's "contrast between § 156 for PTE with the language of § 154 for patent term adjustments." *Novartis v. Ezra*, 909 F.3d at 1373–74. Thus, the rule in *Merck v. Hi-Tech* and *Novartis v. Ezra* for when to apply a PTE does not apply to a PTA because those decisions were premised on the contrast between PTE and PTA.

Third, the statutory language in § 154 is clear that any terminal disclaimer should be applied *after* any PTA (i.e., a PTA cannot adjust a term beyond the expiration date in any disclaimer). 35 U.S.C. § 154(b)(2)(B) ("No patent the term of which has been disclaimed beyond a specified date may be adjusted under this section beyond the expiration date specified in the disclaimer."). Although Appellant asserts that the statute says the term "shall" be extended (Reply Br. 8), Appellant omits that all of those sentences are prefaced with the phrase "Subject to the limitations under paragraph (2)," which includes the limitations due to terminal disclaimers. *Id.* § 154(b)(1)(A), (B), (C). Thus, as recognized by *Merck v. Hi-Tech* and *Novartis v. Ezra*, the statute itself is clear that unlike a PTE under § 156, a PTA under § 154 shall *not* extend the term of a patent past the date of any terminal disclaimer.

Fourth, given that terminal disclaimers arise almost exclusively to overcome obviousness-type double patenting, Congress expressly addressing terminal disclaimers in § 154 is tantamount to addressing obviousness-type double patenting. *See Van Ornum*, 686 F.2d at 948; 37 C.F.R. § 1.321(c), (d); MPEP § 1490(II). Indeed, *Novartis v. Ezra* itself recognized that a rule for terminal disclaimers (from *Merck v. Hi-Tech*) should also apply to obviousness-type double patenting as "a logical extension." 909 F.3d at 1373. The *Novartis v. Ezra* court rejected the argument "that the *Merck* court's rationale only spoke to the impact of a new PTE on preexisting terminal disclaimers," instead finding that the prior "holding on the validity of a PTE for a patent that was terminally disclaimed *in order to overcome an obviousness-type double patenting rejection* is directly relevant to the instant case." *Id.* at 1374 (quotation omitted). Obviousness-type double patenting and terminal disclaimers are two sides of the same coin: the problem and the solution. Just as *Novartis v. Ezra* found a rule on terminal disclaimers was "directly relevant" to double patenting and therefore applied that rule to double patenting as "a logical extension," so too we hold that the statutory rule for terminal disclaimers in § 154 is directly relevant to double patenting and we apply that same rule to double patenting as a logical extension.

Indeed, in this case, Appellant itself argues that double patenting should be applied to post-PTA dates. In particular, Appellant argues that "the '626 Patent cannot be used as an obviousness-type double patenting reference because the '626 Patent expired after the '369 Patent" (Appeal Br. 10 n.1) despite that "the '369 Patent . . . and '626 Patent . . . have the same expiration date except for statutorily-authorized PTA." Appeal Br. 7.

Finally, the Federal Circuit also previously said that "another crucial purpose of the doctrine" of double patenting was "to prevent an inventor from securing a second, later expiring patent" for "[p]atents . . . filed at the same time" that "have different patent terms due to examination delays at the PTO" under "§ 154(b) (patent term adjustments)." *AbbVie Inc. v. Mathilda & Terence Kennedy Inst. of Rheumatology Tr.*, 764 F.3d 1366, 1373 (Fed. Cir. 2014); *see also In re Fallaux*, 564 F.3d 1313, 1319 (Fed. Cir. 2009) ("In some cases there may still be the possibility of an unjust time-wise extension of a patent arising from patent term adjustment under § 154 or patent term extension under § 156."). That is precisely the scenario we have here where two patents have the same effective filing date but expire at different times due solely to PTAs.

Appellant provides no plausible reason for ignoring the clear statutory text and the contrast between § 154 and § 156 that formed the basis of *Merck v. Hi-Tech* and *Novartis v. Ezra*. Nor has Appellant provided any reason for applying the *post*-PTA date for terminal disclaimers yet the *pre*-PTA date for double patenting.[4] We therefore hold that both obviousness-type double patenting and terminal disclaimers should be considered *after* any PTA.[5]

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[4] Applying different dates for double patenting versus terminal disclaimers also creates inconsistent results. For example, suppose the pre-PTA expiration date of Patent A is 1 day after Patent B. Therefore, Patent B could be used as a double patenting reference (pre-PTA) against Patent A, and a terminal disclaimer (post-PTA) would wipe out *all* PTA on Patent A. However, Patent A could *not* be used as a double patenting reference (pre-PTA) against Patent B, so Patent B could have an unlimited amount of PTA, even long after the expiration of Patent A.

[5] 35 U.S.C. § 154(b)(3)(A) gives the Director some discretion "establishing procedures for the application for and determination of patent term

The District Court Decision in Mitsubishi Is Not Persuasive

Appellant also cites a district court decision in *Mitsubishi Tanabe Pharma Corp. v. Sandoz, Inc.*, No. 3:17-cv-05319, __ F. Supp. 3d __, 2021 WL 1845499, at *27–30 (D.N.J. Mar. 22, 2021). Appeal Br. 13–17. We do not find Appellant's citation to *Mitsubishi* persuasive. *See also* Ans. 10.

First, an earlier district court decision in the Western District of Michigan came out the opposite way from *Mitsubishi*. *Magna Elecs., Inc. v. TRW Automotive Holdings Corp.*, No. 12-cv-654, 2015 WL 11430786 (W.D. Mich. Dec. 10, 2015). Although the *Magna Electronics* case appears to have settled prior to any appeal, we understand that the decision in *Mitsubishi* is currently on appeal to the Federal Circuit (No. 21-1876; filed Apr. 23, 2021).

Second, the *Mitsubishi* district court never addressed that double patenting applies even to two patents that have the same filing date, the same issue date, and the same expiration date. *Underwood*, 149 U.S. 224. For example, a terminal disclaimer is still needed to ensure that two patents remain commonly owned. *See Sandy MacGregor Co. v. Vaco Grip Co.*, 2 F.2d 655, 657 (6th Cir. 1924) ("in *Underwood v. Gerber* it was thought that the splitting up of one indivisible right into two and subjecting the infringer to suits by two different owners of the right infringed justified applying the defense of double patenting as against two patents issued on the same day"); *Van Ornum*, 686 F.2d at 945 (similarly summarizing *Underwood*).

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adjustments." Because we decide the case based on the reasoning above, we need not decide whether that discretion includes the PTA issues here.

Third, the district court's entire discussion of the difference between § 154 and § 156 is relegated to a single footnote in which the court does not appear to have understood that a terminal disclaimer is the standard way to cure double patenting, thereby overlooking why the Federal Circuit decided a rule for terminal disclaimers (*Merck v. Hi-Tech*) should also apply to a double patenting analysis (*Novartis v. Ezra*) as a "logical extension." *See Mitsubishi*, 2021 WL 1845499, at *29 n.45.

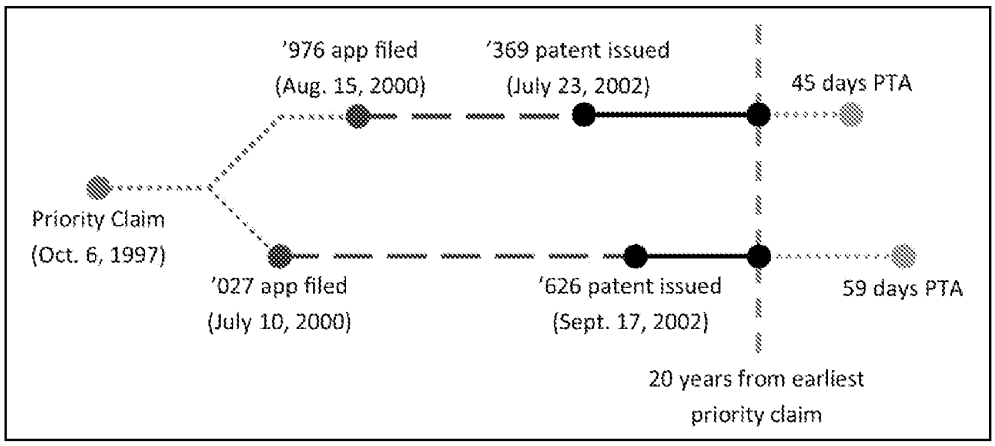
Fourth, even within the same paragraph, the district court confuses when the challenged patent would have expired relative to the reference patent. *Compare Mitsubishi*, 2021 WL 1845499, at *29 ("absent the PTA granted to the '788 Patent, both the '788 Patent and the '219 Patent would have the same expiration date"), *with id.* ("but for the § 154(b) PTA, the '788 Patent would have expired before the '219 Patent"). So it is not clear whether the district court was even considering the right facts.

For these reasons, we give little weight to the *Mitsubishi* decision.

The '626 Patent Is Not a Valid Reference for Double Patenting

Appellant argues that "the '626 Patent cannot be used as an obviousness-type double patenting reference because the '626 Patent expired after the '369 Patent." Appeal Br. 10.

We agree with Appellant. The timeline below shows the relevant dates for the '369 patent (on top) and '626 patent (on bottom):



Timeline for expiration of '369 patent (top) & '626 patent (bottom)

As clearly illustrated in the timeline, the challenged patent (the '369 patent) and the '626 patent (one of the two reference patents) come from the same patent family and claim priority to the same date (October 6, 1997). However, the '626 patent expired *after* the challenged patent due to having more PTA (59 days vs. 45 days). For two patents with different expiration dates, double patenting only invalidates the later patent, whereas here the challenged patent is the *earlier* patent and the '626 patent is the *later* patent.

Even if we were to consider double patenting before applying any PTA, the pre-PTA expiration date of the '626 patent and the challenged patent is the same day yet the '626 patent issued *after* the challenged patent, so the '626 patent still would be the *second* patent and therefore not eligible as a double patenting reference against the *first* patent.

The Examiner appears to rely on the claims of the '626 patent not being entitled to the 1997 priority date due to intervening continuations-in-part. *See* Ans. 8–10. However, we agree with Appellant that "Title 35 is clear that patent term runs from the earliest [non-provisional U.S.] filing date to which priority is claimed," and the "term is not affected by whether or not

the priority application actually supports . . . [the] claims." Appeal Br. 6, 9–10. By statute, the only question for an expiration date is "if the application *contains a specific reference to* an earlier filed application" under 35 U.S.C. §§ 120, 121, 365(c), or 386(c). 35 U.S.C. § 154(a)(2) (emphasis added). The statute does not require that any claim actually be entitled to that earlier date. *See Nat. Alternatives Int'l, Inc. v. Iancu*, 904 F.3d 1375, 1383 (Fed. Cir. 2018) ("the standard patent term is twenty years after an application's *earliest-claimed* priority date," even if "claims reciting new matter are not entitled to the parent application's earlier filing date"). Here, the '626 patent contains a specific reference to the earlier "application No. 08/944,322, filed on Oct. 6, 1997, now Pat. No. 5,929,901" as a continuation-in-part under § 120, which is all that is required by § 154(a)(2). '626 patent, code (63), 1:5–13.

We therefore do not sustain the rejection over the '626 patent.

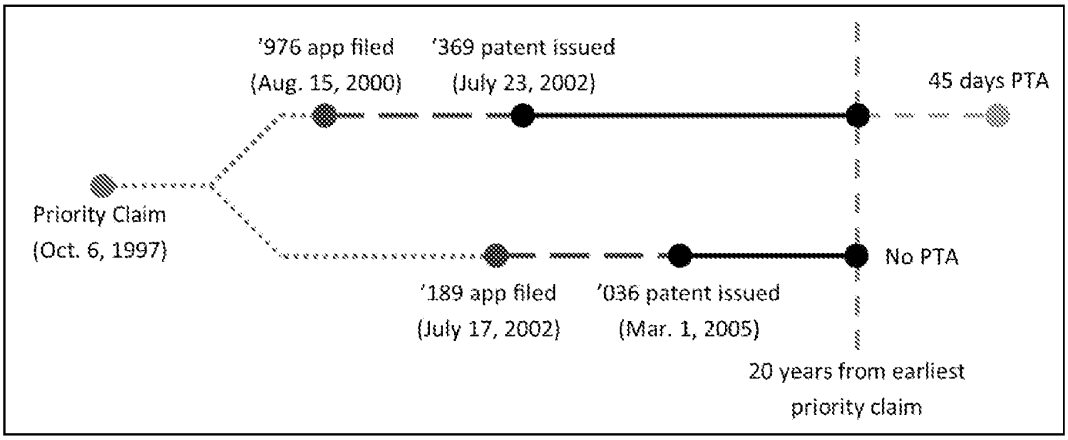
Overview of the '036 Patent Rejection

We next turn to the rejection over the '036 patent. Although the challenged patent (the '369 patent) issued before the '036 patent, both patents again come from the same patent family and both claim priority to the same application (filed Oct. 6, 1997) so they normally would expire at the same time (Oct. 6, 2017).[6] 35 U.S.C. § 154(a)(2). However, due to

[6] We need not address Appellant's argument over whether the claims of the '369 patent are actually entitled to the 1997 date. Appeal Br. 23–25. As discussed above for the '626 patent, expiration is based on a priority date "if the application *contains a specific reference to an earlier filed application*," regardless whether any claim is actually entitled to that priority date. 35 U.S.C. § 154(a)(2) (emphasis added).

various delays by the USPTO during prosecution, the '369 patent was granted a patent term adjustment ("PTA") under 35 U.S.C. § 154(b) of 45 days, whereas the '036 patent did not receive any PTA. Therefore, the '036 patent expired *before* the challenged patent. Both patents are now expired, but the statute of limitations for past damages has not yet passed. 35 U.S.C. § 286.

The timeline below shows the relevant dates for the two patents, including priority, filing, issuance, expiration, and PTA, with the challenged patent on top and the '036 patent below:



Timeline for expiration of '369 patent (top) & '036 patent (bottom)

In this reexamination, the examiners invoked the doctrine of obviousness-type double patenting to reject the claims of the challenged patent as obvious variants of claims in the '036 patent. Final Act. 5–39. Appellant does not dispute that the claims of the '036 patent would have rendered obvious the claims of the challenged patent. Instead, Appellant argues the '036 patent cannot be used for double patenting because (1) a judicially-created doctrine cannot take away statutorily guaranteed time, especially in light of the Federal Circuit's treatment of patent term

extensions ("PTE") under 35 U.S.C. § 156, (2) the result would be inequitable given the facts here, and (3) no substantial new question of patentability has been raised because the examiner should have considered double patenting in the original prosecution. *See* Appeal Br. 4–23.

We are not persuaded by Appellant's arguments. First, unlike a PTE under § 156, the statute for a PTA (§ 154) states that any terminal disclaimer should be applied *after* any PTA. Because the primary purpose of a terminal disclaimer is to overcome double patenting, the same rule should apply to double patenting. Second, the result here is not inequitable because the Federal Circuit has said the existence of any extra term of a second patent is itself what is inequitable, and Appellant still enjoyed the entire term of the earliest patent. Third, double patenting is a substantial new question because, regardless of what should have happened in the original prosecution, there is insufficient evidence that the original examiner actually considered double patenting.

Double Patenting Here Was Proper

As discussed above, we hold that double patenting should be considered *after* any PTA is applied. Here, after applying the PTA, the challenged patent expired after the '036 patent due to the challenged patent having 45 days of PTA beyond the expiration date of the '036 patent. Appeal Br. 11. Thus, the later-expiring claims of the challenged patent were properly rejected for obviousness-type double patenting over the earlier-expiring claims of the '036 patent.

Appellant does argue that "there has been no harassment by multiple assignees" because the patents have been commonly owned so far and the

patents are now expired. Appeal Br. 13. But the statutory time limitation for past damages is "six years prior to the filing of the complaint." 35 U.S.C. § 286. The patents here expired less than six years ago, so the risk still remains for multiple assignees to seek past damages. Indeed, Appellant has already filed one lawsuit after both patents expired. Appeal Br. 2.

Appellant further argues that the patents "will be maintained by the same owner." Appeal Br. 13. The only basis for this assertion is a single paragraph from a declaration of one inventor:

> Because of the exclusive (field-of-use) nature of certain license agreements, MIS/Cellect may not freely assign these patents and they have been, and will continue to be, owned by MIS/Cellect. As the Chief Technology Officer and Co-Founder of Micro Imaging Solutions LLC, I can confirm that MIS/Cellect will not sell off or split apart any portion of the patents that comprise the '369 Patent family to a third-party.

Adair Decl. ¶ 24 (Sept. 30, 2020). But such a declaration is unpersuasive. For example, suppose Appellant went out of business and a bankruptcy court (not Appellant itself) split the patents among various creditors. Even if Appellant's licensees might have a breach-of-contract claim against the new patent owners, a third party sued by the multiple new owners has no way to enforce the inventor's declaration absent double patenting.

There also is no need to wait until *actual* harassment by multiple assignees. *See* Appeal Br. 9 ("this judicially created doctrine requires . . . harassment by multiple assignees"). One goal of double patenting and terminal disclaimers is to preemptively prevent the risk of such harassment:

> Even though both patents are issued to the same patentee or assignee, it (is) possible that ownership of the two will be divided by later transfers and assignments. The possibility of multiple suits against an infringer by assignees of related patents has long

> been recognized as one of the concerns behind the doctrine of double patenting.

Van Ornum, 686 F.2d at 944 (quoting Chisum on Patents § 9.04(2)(b) (1981)).

In sum, the double patenting rejection here was proper because any PTA is applied before the double patenting analysis and here the challenged patent's post-PTA expiration date is after that of the '036 patent.

Substantial New Question

Appellant argues there is no substantial new question of patentability because the examiner in the original prosecution was aware of both applications and "conducted an interference search" for both, so the examiner "would have" made a double patenting rejection "if [the examiner] believed that such a rejection was warranted." Appeal Br. 12, 22–23.

We are not persuaded by Appellant's arguments. A substantial new question of patentability does exist here because there is insufficient evidence that double patenting actually was considered during the original prosecution. Ans. 14–15. Regardless of what ideally should have happened during the original prosecution, the reexamination process exists because items sometimes get overlooked or errors are made. *See, e.g.*, *Patlex Corp. v. Mossinghoff*, 758 F.2d 594, 604 (Fed. Cir. 1985) ("The reexamination statute's purpose is to correct errors made by the government . . . and if need be to remove patents that should never have been granted."), *on reh'g*, 771 F.2d 480, 481 (Fed. Cir. 1985) (denying the petition in relevant part).

Equity

Appellant argues that "an equitable doctrine should not be applied in a manner that would be inequitable" given that "filing a terminal disclaimer now is not possible as the patents are expired" and "the record is completely devoid" of any "gamesmanship" or "unjustified or improper timewise extension." Appeal Br. 21–22 (quotation omitted).

However, the Federal Circuit is unambiguous that the inequity here is Appellant's enjoyment of a second patent's term beyond the expiration of the first patent:

> When the claims of a patent are obvious in light of the claims of an earlier commonly owned patent, the patentee can have no right to exclude others from practicing the invention encompassed by the later patent after the date of the expiration of the earlier patent. But when a patentee does not terminally disclaim the later patent before the expiration of the earlier related patent, the later patent purports to remain in force even after the date on which the patentee no longer has any right to exclude others from practicing the claimed subject matter. By permitting the later patent to remain in force beyond the date of the earlier patent's expiration, the patentee wrongly purports to inform the public that it is precluded from making, using, selling, offering for sale, or importing the claimed invention during a period after the expiration of the earlier patent.
>
> By failing to terminally disclaim a later patent prior to the expiration of an earlier related patent, a patentee enjoys an unjustified advantage—a purported time extension of the right to exclude from the date of the expiration of the earlier patent. The patentee cannot undo this unjustified timewise extension by retroactively disclaiming the term of the later patent because it has *already* enjoyed rights that it seeks to disclaim.

Boehringer, 592 F.3d at 1347–48 (citations omitted); *see also Lonardo*, 119 F.3d at 965. Appellant also never addresses preserving the public's right to make what is covered by the *earlier* patent after it expired:

> The bar against double patenting was created to preserve that bargained-for right held by the public. *See, e.g., Miller v. Eagle Mfg. Co.*, 151 U.S. 186, 197–98, 202 (1894); . . . *Odiorne v. Amesbury Nail Factory*, 18 F.Cas. 578, 579 (C.C.D.Mass.1819). If an inventor could obtain several sequential patents on the same invention, he could retain for himself the exclusive right to exclude or control the public's right to use the patented invention far beyond the term awarded to him under the patent laws. As Justice Story explained in 1819, "[i]t cannot be" that a patentee can obtain two patents in sequence "substantially for the same invention[] and improvements"; "it would completely destroy the whole consideration derived by the public for the grant of the patent, viz. the right to use the invention at the expiration of the term." *Odiorne*, 18 F.Cas. at 579. Thus, the doctrine of double patenting was primarily designed to prevent such harm by limiting a patentee to one patent term per invention or improvement.

Gilead, 753 F.3d at 1212 (parallel citations omitted).

Even beyond the mere existence of the extra term, Appellant concedes that it actively filed at least one lawsuit on the challenged patent after the expiration of both patents, yet Appellant fails to address whether that lawsuit seeks damages for the extra term of the challenged patent. *See* Appeal Br. 2.

Moreover, invalidating the challenged claims of a *second* patent (or third, fourth, and fifth patents in the case of the numerous related reexaminations here) does not take away Appellant's right to enforce its *first* patent.

Thus, Appellant fails to persuade us that the result here is inequitable.

Conclusion on '036 Patent Rejection

Accordingly, we sustain the double patenting rejection of claims 1, 17, 19, 21, 22, 27, 49, 55, and 61 over certain claims of the '036 Patent and Tran.

OUTCOME

The following table summarizes the outcome of the rejection:

Claim(s) Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1, 17, 19, 21, 22, 27, 49, 55, 61		Double patenting: '036 patent and Tran	1, 17, 19, 21, 22, 27, 49, 55, 61	
1, 17, 19, 21, 22, 27, 49, 55, 61		Double patenting: '626 patent and APA		1, 17, 19, 21, 22, 27, 49, 55, 61
Overall Outcome			1, 17, 19, 21, 22, 27, 49, 55, 61	

TIME TO RESPOND

Requests for extensions of time in this *ex parte* reexamination proceeding are governed by 37 C.F.R. § 1.550(c). *See* 37 C.F.R. § 41.50(f).

AFFIRMED

cc Third Party Requester:

KRAMER LEVIN NAFTALIS & FRANKEL LLP
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31013 7590 12/01/2021

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GE, YUZHEN

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The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte Cellect LLC
Patent Owner and Appellant

Appeal 2021-005046
Reexamination Control 90/014,455
Patent 6,452,626 B1
Technology Center 3900

Before ALLEN R. MacDONALD, GARTH D. BAER, and MICHAEL J. ENGLE, *Administrative Patent Judges*.

ENGLE, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. §§ 134(b) and 306, Appellant[1] appeals from the rejection of claims 1, 5, 11, 33, 34, 58, and 64 of U.S. Patent No. 6,452,626 B1 ("the '626 patent" or "challenged patent") in this *ex parte* reexamination. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

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[1] Appellant states that the real party in interest is "Cellect LLC, a wholly owned subsidiary of Micro Imaging Solutions LLC." Appeal Br. 2.

TECHNOLOGY

The application relates to "solid state image sensors which are configured to be of a minimum size and used within communication devices specifically including video telephones." '626 patent, 1:16–20.

RELATED MATTERS

The challenged patent and its patent family have been involved in a number of proceedings before federal district courts and the USPTO. Appeal Br. 2–3 (listing 1 district court case, 20 *inter partes* review petitions, and 5 *ex parte* reexamination requests); Final Act. 4 (listing another district court case). Four of the reexaminations involve substantially similar issues on double patenting. *See* Appeal Nos. 2021-005046; 2021-005258; 2021-005302; 2021-005303.

For the challenged patent, three petitions for *inter partes* review were denied institution because "the scope of [the] challenged claims . . . is uncertain." IPR2020-00565, Paper 14, at 17 (Oct. 5, 2020); IPR2020-00566, Paper 14, at 17 (Oct. 5, 2020); IPR2020-00567, Paper 14, at 17 (Oct. 5, 2020). As it was not raised in the present proceeding, we do not address indefiniteness here.

REJECTIONS

Claims 1, 5, 11, 33, 34, 58, and 64 are rejected for non-statutory double patenting over claims 14, 5, 11, 46, 34, 58, and 64 of U.S. Patent No. 6,424,369 ("the '369 patent" or "reference patent"). Final Act. 8–20.

Claims 1, 5, 11, 33, 34, 58, and 64 are rejected for non-statutory double patenting over claims 14, 5, 11, 46, 34, 58, and 64 of the '369 patent in view of Nguyen (WO 97/09813; Mar. 13, 1997). Final Act. 20–22.

ISSUE

Did the Examiner err in applying an obviousness-type double patenting rejection to two related patents that (1) claim the same priority date, (2) have different patent term adjustments, and (3) are expired?

ANALYSIS

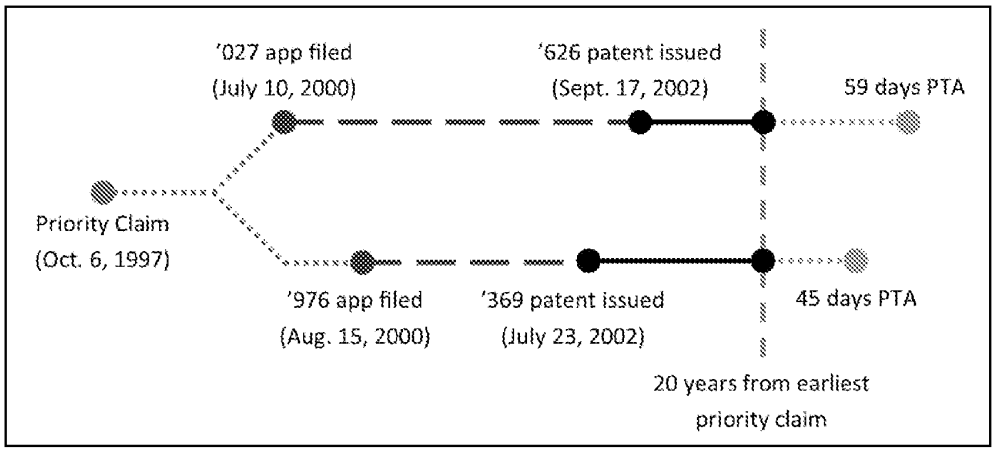
Overview

The challenged patent (the '626 patent) and the reference patent (the '369 patent) belong to the same patent family. The challenged patent issued after the reference patent, but both claim priority to the same application (filed Oct. 6, 1997) so they normally would expire at the same time (Oct. 6, 2017).[2] 35 U.S.C. § 154(a)(2). However, due to various delays by the USPTO during prosecution, both were granted a patent term adjustment ("PTA") under 35 U.S.C. § 154(b), with the challenged patent receiving more PTA than the reference patent (59 days vs. 45 days). Therefore, the reference patent expired *before* the challenged patent. Both patents are now expired, but the statute of limitations for past damages has not yet passed. 35 U.S.C. § 286.

The timeline below shows the relevant dates for the two patents, including priority, filing, issuance, expiration, and PTA, with the challenged patent on top and the reference patent below:

---

[2] We agree with the Examiner that whether the claims are actually entitled to the claimed date is not relevant to a double patenting analysis. Ans. 5; Appeal Br. 17–21. By statute, expiration is based on a priority date "if the application *contains a specific reference to an earlier filed application*," regardless whether any claim is actually entitled to that priority date. 35 U.S.C. § 154(a)(2) (emphasis added).



Timeline for expiration of '626 patent (top) & '369 patent (bottom)

In this reexamination, the examiners invoked the doctrine of obviousness-type double patenting to reject the claims of the challenged patent as obvious variants of claims in the reference patent, either alone or in combination with Nguyen. Final Act. 7–22. Appellant does not dispute that the claims of the reference patent would have rendered obvious the claims of the challenged patent. Instead, Appellant argues the reference patent cannot be used for double patenting because (1) a judicially-created doctrine cannot take away statutorily guaranteed time, especially in light of the Federal Circuit's treatment of patent term extensions ("PTE") under 35 U.S.C. § 156, (2) the result would be inequitable given the facts here, and (3) no substantial new question of patentability has been raised because the examiner should have considered double patenting in the original prosecution. *See* Appeal Br. 4–17.

We are not persuaded by Appellant's arguments. First, unlike a PTE under § 156, the statute for a PTA (§ 154) states that any terminal disclaimer should be applied *after* any PTA. Because the primary purpose of a terminal disclaimer is to overcome double patenting, the same rule should apply to

double patenting. Moreover, even if double patenting was based on the expiration date *before* applying any PTA (akin to a PTE), double patenting still would be appropriate here because two patents that are obvious variants and expire on the same day still need a terminal disclaimer to enforce common ownership. Second, the result here is not inequitable because the Federal Circuit has said the existence of any extra term of a second patent is itself what is inequitable, and Appellant still enjoyed the entire term of the earliest patent. Third, double patenting is a substantial new question because, regardless of what should have happened in the original prosecution, there is insufficient evidence that the original examiner actually considered double patenting.

Standard of Review

The PTO is "authorized during reexamination to consider the question of double patenting." *In re Lonardo*, 119 F.3d 960, 966 (Fed. Cir. 1997); *see also* MPEP § 2258(I)(D); Ans. 6–7. "As with statutory obviousness under 35 U.S.C. § 103, obviousness-type double patenting is an issue of law premised on underlying factual inquiries." *Eli Lilly & Co. v. Teva Parenteral Meds., Inc.*, 689 F.3d 1368, 1376 (Fed. Cir. 2012).

Legal Background
on Obviousness-Type Double Patenting, Terminal Disclaimers, PTA, & PTE

Obviousness-type double patenting is a "judicially created" doctrine that "prohibits an inventor from obtaining a second patent for claims that are not patentably distinct from the claims of the first patent." *Lonardo*, 119 F.3d at 965. "There are two justifications for obviousness-type double patenting": (1) "to prevent unjustified timewise extension of the right to

exclude granted by a patent no matter how the extension is brought about" and (2) "to prevent multiple infringement suits by different assignees asserting essentially the same patented invention." *In re Hubbell*, 709 F.3d 1140, 1145 (Fed. Cir. 2013) (quotation omitted). For example, if an inventor receives a second patent with claims that are merely obvious variants of a first patent, double patenting helps prevent the patentee from (1) suing on the second patent after the first has already expired (i.e., improper time-wise extension) or (2) selling the two patents to different entities only to have both entities separately sue an alleged infringer on two obvious variants of each other (i.e., improper harassment by multiple assignees).

A patentee or applicant often can overcome double patenting by filing a terminal disclaimer. *Boehringer Ingelheim Int'l GmbH v. Barr Labs., Inc.*, 592 F.3d 1340, 1346 (Fed. Cir. 2010). Terminal disclaimers are expressly permitted by statute to "disclaim or dedicate to the public . . . any terminal part of the term" of a patent. 35 U.S.C. § 253(b). The USPTO has provided regulations on what a terminal disclaimer must contain to be effective. *E.g.*, 37 C.F.R. § 1.321. A terminal disclaimer solves the two concerns of double patenting by (1) making the *later* patent expire with the *earlier* patent and (2) rendering the second patent unenforceable if it is not commonly owned with the first patent. *E.g.*, 37 C.F.R. § 1.321(b)(2), (c)(3), (d)(3); MPEP §§ 804.02(VI), 1490(VI)(A), (IX). However, "a terminal disclaimer filed after the expiration of the earlier patent over which claims have been found obvious cannot cure obviousness-type double patenting." *Boehringer*, 592 F.3d at 1347–48. Thus, a terminal disclaimer cannot cure any double patenting rejection against the expired patents here. Appeal Br. 9.

For two issued patents, double patenting and the need for a terminal disclaimer generally only apply to the *later* patent.[3] *See Eli Lilly & Co. v. Barr Labs., Inc.*, 251 F.3d 955, 968 & n.5 (Fed. Cir. 2001) ("A *later* claim that is not patentably distinct from an earlier claim in a commonly owned patent is invalid for obvious-type double patenting."; "A patent owner cannot avoid double patenting by disclaiming the *earlier* patent." (emphases added)). The question then is how to determine which patent is "later." The answer depends on whether the patents issued from applications filed on or after June 8, 1995. This date is six months after enactment of the Uruguay Round Agreements Act ("URAA"), which changed the term of a patent from (A) 17 years after issue to (B) 20 years from the earliest filing date of any non-provisional U.S. application to which that patent claims priority. 35 U.S.C. § 154.

For two post-URAA patents, the "later" patent generally is determined by looking at the *expiration* date. *Novartis Pharms. Corp. v. Breckenridge Pharm. Inc.*, 909 F.3d 1355, 1362–63, 1366 (Fed. Cir. 2018). For two pre-URAA patents or certain scenarios involving one patent on each side of the URAA date, the "later" patent is instead determined by looking at the *issue* date. *Id.* at 1362 ("Traditionally, courts looked at the issuance dates of the respective patents, because, under the law pre-URAA, the expiration date of the patent was inextricably intertwined with the issuance date, and used the earlier-issued patent to limit the patent term(s) of the later issued

[3] For two co-pending applications, a provisional double patenting rejection against both applications may be appropriate if it is not yet known which will result in the later patent. *See* MPEP § 804(I)(1).

patent(s)."). Prior to the URAA, a patent expired 17 years after issuance, so "looking to patent issue dates had previously served as a reliable stand-in for the date that really mattered—patent expiration." *Gilead Scis., Inc. v. Natco Pharma Ltd.*, 753 F.3d 1208, 1215 (Fed. Cir. 2014). Finally, if two post-URAA patents expire on the same day or two pre-URAA patents have the same issue date, then the patent with the higher patent number may be invalid for double patenting.[4] *See Underwood v. Gerber*, 149 U.S. 224 (1893) (affirming Patent No. 348,073 was void over the same inventors' Patent No. 348,072 when both patents had the same filing date, issue date, and expiration date).

A complication arises, however, in that Congress also provided two ways to potentially prolong the term of a patent. A patent term adjustment ("PTA") under § 154(b) may adjust the term based on certain delays by the USPTO during prosecution, and a patent term extension ("PTE") under § 156 may extend the term based on certain regulatory delays, such as the FDA reviewing a new drug. 35 U.S.C. §§ 154(b), 156. The question before us now is how a PTA under § 154 should factor into the double patenting analysis, such as whether double patenting should be based on the expiration date *before* a PTA or *after*. The Federal Circuit already addressed similar questions for a PTE, yet it did so by contrasting the statutes for PTE (§ 156) versus PTA (§ 154). We discuss these cases below.

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[4] As the patents here issued on different dates, we need not resolve whether an analysis for patents issued on the same day should first look to priority date or filing date rather than patent number (e.g., two pre-URAA patents with the same issue date but the patent with the higher patent number has a significantly earlier filing date and priority date).

PTE & Terminal Disclaimers
(Merck v. Hi-Tech)

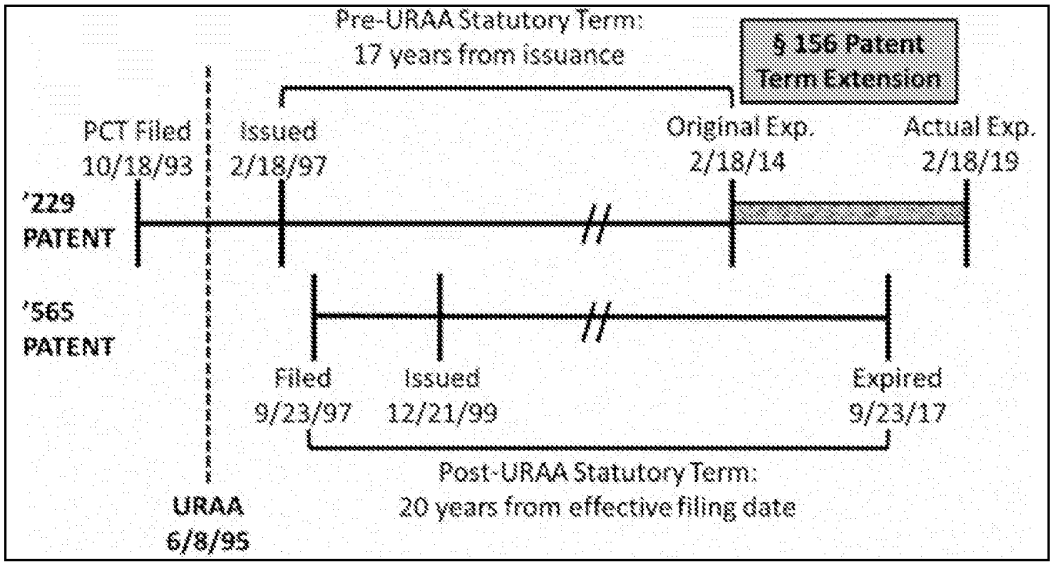
For a PTE under § 156, the starting point is *Merck & Co. v. Hi-Tech Pharmacal Co.*, 482 F.3d 1317 (Fed. Cir. 2007). In that case, the patent owner had already filed a terminal disclaimer to overcome an obviousness-type double patenting rejection. 482 F.3d at 1318–19. Later, the patent was awarded a PTE under § 156. *Id.* at 1319. The question before the court was whether a PTE under § 156 could be applied to a patent subject to a terminal disclaimer. *Id.* at 1324. The court held "a patent term extension under § 156 is not foreclosed by a terminal disclaimer." *Id.* at 1322. In particular, "[t]he computation of a Hatch–Waxman patent term extension is from the expiration date resulting from the terminal disclaimer and not from the date the patent would have expired in the absence of the terminal disclaimer." *Id.* at 1322–23. Put another way, a PTE under § 156 is applied *after* any terminal disclaimer.

The Federal Circuit reached this conclusion by contrasting PTE with PTA. For a PTA, "§ 154(b)(2)(B) expressly excludes patents in which a terminal disclaimer was filed from the benefit of a term adjustment for PTO delays." *Merck v. Hi-Tech*, 482 F.3d at 1322. Specifically, the statute states that "[n]o patent the term of which has been disclaimed beyond a specified date may be adjusted under this section beyond the expiration date specified in the disclaimer." 35 U.S.C. § 154(b)(2)(B). The Federal Circuit explained that "[t]here is no similar provision that excludes patents in which a terminal disclaimer was filed from the benefits of Hatch-Waxman extensions" under § 156. *Merck v. Hi-Tech*, 482 F.3d at 1322. Thus, a terminal disclaimer is applied *before* a PTE *because* PTE is different than PTA.

PTE & Double Patenting
(Novartis v. Ezra)

The next question was how a PTE applied to double patenting in the absence of a terminal disclaimer. As noted above, a terminal disclaimer generally is filed to overcome obviousness-type double patenting. *In re Van Ornum*, 686 F.2d 937, 948 (CCPA 1982); 37 C.F.R. § 1.321(c), (d); MPEP § 1490(II). Given this relationship between double patenting and terminal disclaimers and given the holding in *Merck v. Hi-Tech* that a terminal disclaimer applies *before* a PTE, the Federal Circuit not surprisingly held "as a logical extension of our holding in *Merck & Co. v. Hi-Tech*" that double patenting also should be considered *before* a PTE. *Novartis AG v. Ezra Ventures LLC*, 909 F.3d 1367, 1373–74 (Fed. Cir. 2018). Thus, "if a patent, under its original expiration date without a PTE, should have been (but was not) terminally disclaimed because of obviousness-type double patenting, then this court's obviousness-type double patenting case law would apply, and the patent could be invalidated." *Id.* at 1374. "However, if a patent, under its pre-PTE expiration date, is valid under all other provisions of law, then it is entitled to the full term of its PTE." *Id.*

A timeline for the patents in *Novartis v. Ezra* is reproduced below:



Novartis v. Ezra, 909 F.3d at 1370. As shown in the timeline above, the challenged patent (the '229 patent) had an *earlier* filing date, issue date, and pre-PTE expiration date than the reference patent (the '565 patent). Because the challenged patent was the *earlier* patent (at least pre-PTE), the challenged patent was not invalid for double patenting. *Id.* at 1373–75.

PTA & Double Patenting

The question now before us is how a PTA affects double patenting. Appellant relies on one broadly worded sentence in *Novartis v. Ezra* to argue that "a judge-made doctrine" (i.e., obviousness-type double patenting) cannot "cut off a statutorily-authorized time extension." Appeal Br. 11 (quoting *Novartis v. Ezra*, 909 F.3d at 1375). Although the holding in *Novartis v. Ezra* was about a PTE under § 156, Appellant extends that argument to suggest that any PTA under § 154 also is a "statutory grant of additional term" that "cannot be deemed improper." *Id.*

Appellant's argument is not persuasive because it ignores the plain text of § 154 and the actual holding in *Novartis v. Ezra*.

First, contrary to Appellant's assertions, the decision in *Novartis v. Ezra* reaffirms that a double patenting analysis *should* be done even if a patent has a PTE. The real question was whether double patenting should be considered *before* or *after* a PTE, with the court ultimately deciding double patenting should be considered *before* a PTE. *Novartis v. Ezra*, 909 F.3d at 1374 ("if a patent, under its original expiration date without a PTE, should have been (but was not) terminally disclaimed because of obviousness-type double patenting, then this court's obviousness-type double patenting case law would apply, and the patent could be invalidated"). So here, we must do a double patenting analysis and the question is whether double patenting should be considered with the expiration dates *before* or *after* a PTA.

Second, the outcome for a PTE under § 156 in *Merck v. Hi-Tech* was based on the difference between § 156 and § 154. In particular, "§ 154(b)(2)(B) expressly excludes patents in which a terminal disclaimer was filed from the benefit of a term adjustment for PTO delays," but there is an "absence of any such prohibition regarding Hatch–Waxman extensions" under § 156. *Merck v. Hi-Tech*, 482 F.3d at 1322. That reasoning in *Merck v. Hi-Tech* was important enough that when summarizing the prior case, *Novartis v. Ezra* repeated the prior case's "contrast between § 156 for PTE with the language of § 154 for patent term adjustments." *Novartis v. Ezra*, 909 F.3d at 1373–74. Thus, the rule in *Merck v. Hi-Tech* and *Novartis v. Ezra* for when to apply a PTE does not apply to a PTA because those decisions were premised on the contrast between PTE and PTA.

Third, the statutory language in § 154 is clear that any terminal disclaimer should be applied *after* any PTA (i.e., a PTA cannot adjust a term beyond the expiration date in any disclaimer). 35 U.S.C. § 154(b)(2)(B) ("No patent the term of which has been disclaimed beyond a specified date may be adjusted under this section beyond the expiration date specified in the disclaimer."). Although Appellant asserts that the statute says the term "shall" be extended (Reply Br. 6–7), Appellant omits that all of those sentences are prefaced with the phrase "Subject to the limitations under paragraph (2)," which includes the limitations due to terminal disclaimers. *Id.* § 154(b)(1)(A), (B), (C). Thus, as recognized by *Merck v. Hi-Tech* and *Novartis v. Ezra*, the statute itself is clear that unlike a PTE under § 156, a PTA under § 154 shall *not* extend the term of a patent past the date of any terminal disclaimer.

Fourth, given that terminal disclaimers arise almost exclusively to overcome obviousness-type double patenting, Congress expressly addressing terminal disclaimers in § 154 is tantamount to addressing obviousness-type double patenting. *See Van Ornum*, 686 F.2d at 948; 37 C.F.R. § 1.321(c), (d); MPEP § 1490(II). Indeed, *Novartis v. Ezra* itself recognized that a rule for terminal disclaimers (from *Merck v. Hi-Tech*) should also apply to obviousness-type double patenting as "a logical extension." 909 F.3d at 1373. The *Novartis v. Ezra* court rejected the argument "that the *Merck* court's rationale only spoke to the impact of a new PTE on preexisting terminal disclaimers," instead finding that the prior "holding on the validity of a PTE for a patent that was terminally disclaimed *in order to overcome an obviousness-type double patenting rejection* is directly relevant to the instant

case." *Id.* at 1374 (quotation omitted). Obviousness-type double patenting and terminal disclaimers are two sides of the same coin: the problem and the solution. Just as *Novartis v. Ezra* found a rule on terminal disclaimers was "directly relevant" to double patenting and therefore applied that rule to double patenting as "a logical extension," so too we hold that the statutory rule for terminal disclaimers in § 154 is directly relevant to double patenting and we apply that same rule to double patenting as a logical extension.

Indeed, in at least one related reexamination, Appellant itself argues that double patenting should be applied to post-PTA dates. *Compare* Appeal 2021-005302, Appeal Br. 7 ("the '369 Patent . . . and '626 Patent . . . have the same expiration date except for statutorily-authorized PTA"), *with id.* at 10 n.1 ("the '626 Patent cannot be used as an obviousness-type double patenting reference because the '626 Patent expired after the '369 Patent"). That case applied the same two patents at issue here, just with the roles reversed (i.e., the '626 patent as the reference patent against the '369 patent).

Finally, the Federal Circuit also previously said that "another crucial purpose of the doctrine" of double patenting was "to prevent an inventor from securing a second, later expiring patent" for "[p]atents . . . filed at the same time" that "have different patent terms due to examination delays at the PTO" under "§ 154(b) (patent term adjustments)." *AbbVie Inc. v. Mathilda & Terence Kennedy Inst. of Rheumatology Tr.*, 764 F.3d 1366, 1373 (Fed. Cir. 2014); *see also In re Fallaux*, 564 F.3d 1313, 1319 (Fed. Cir. 2009) ("In some cases there may still be the possibility of an unjust time-wise extension of a patent arising from patent term adjustment under § 154 or patent term extension under § 156."). That is precisely the scenario

we have here where two patents have the same effective filing date but expire at different times due solely to PTAs.

Appellant provides no plausible reason for ignoring the clear statutory text and the contrast between § 154 and § 156 that formed the basis of *Merck v. Hi-Tech* and *Novartis v. Ezra*. Nor has Appellant provided any reason for applying the *post*-PTA date for terminal disclaimers yet the *pre*-PTA date for double patenting.[5] We therefore hold that both obviousness-type double patenting and terminal disclaimers should be considered *after* any PTA.[6]

The District Court Decision in Mitsubishi Is Not Persuasive

Appellant also cites a district court decision in *Mitsubishi Tanabe Pharma Corp. v. Sandoz, Inc.*, No. 3:17-cv-05319, __ F. Supp. 3d __, 2021 WL 1845499, at *27–30 (D.N.J. Mar. 22, 2021). Supp. Br. 13–17 (Mar. 29, 2021).[7] We do not find Appellant's citation to *Mitsubishi* persuasive. *See also* Ans. 19.

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[5] Applying different dates for double patenting versus terminal disclaimers also creates inconsistent results. For example, suppose the pre-PTA expiration date of Patent A is 1 day after Patent B. Therefore, Patent B could be used as a double patenting reference (pre-PTA) against Patent A, and a terminal disclaimer (post-PTA) would wipe out *all* PTA on Patent A. However, Patent A could *not* be used as a double patenting reference (pre-PTA) against Patent B, so Patent B could have an unlimited amount of PTA, even long after the expiration of Patent A.

[6] 35 U.S.C. § 154(b)(3)(A) gives the Director some discretion "establishing procedures for the application for and determination of patent term adjustments." Because we decide the case based on the reasoning above, we need not decide whether that discretion includes the PTA issues here.

[7] The *Mitsubishi* decision (Mar. 22, 2021) was issued after the Appeal Brief had already been filed (Feb. 16, 2021), so Appellant raised it in a

First, an earlier district court decision in the Western District of Michigan came out the opposite way from *Mitsubishi*. *Magna Elecs., Inc. v. TRW Automotive Holdings Corp.*, No. 12-cv-654, 2015 WL 11430786 (W.D. Mich. Dec. 10, 2015). Although the *Magna Electronics* case appears to have settled prior to any appeal, we understand that the decision in *Mitsubishi* is currently on appeal to the Federal Circuit (No. 21-1876; filed Apr. 23, 2021).

Second, the *Mitsubishi* district court never addressed that double patenting applies even to two patents that have the same filing date, the same issue date, and the same expiration date. *Underwood*, 149 U.S. 224. For example, a terminal disclaimer is still needed to ensure that two patents remain commonly owned. *See Sandy MacGregor Co. v. Vaco Grip Co.*, 2 F.2d 655, 657 (6th Cir. 1924) ("in *Underwood v. Gerber* it was thought that the splitting up of one indivisible right into two and subjecting the infringer to suits by two different owners of the right infringed justified applying the defense of double patenting as against two patents issued on the same day"); *Van Ornum*, 686 F.2d at 945 (similarly summarizing *Underwood*).

Third, the district court's entire discussion of the difference between § 154 and § 156 is relegated to a single footnote in which the court does not appear to have understood that a terminal disclaimer is the standard way to cure double patenting, thereby overlooking why the Federal Circuit decided a rule for terminal disclaimers (*Merck v. Hi-Tech*) should also apply to a

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"Supplemental Submission of New Authority Pursuant to MPEP 1205.02" ("Supp. Br.") dated March 29, 2021.

double patenting analysis (*Novartis v. Ezra*) as a "logical extension." *See Mitsubishi*, 2021 WL 1845499, at *29 n.45.

Fourth, even within the same paragraph, the district court confuses when the challenged patent would have expired relative to the reference patent. *Compare Mitsubishi*, 2021 WL 1845499, at *29 ("absent the PTA granted to the '788 Patent, both the '788 Patent and the '219 Patent would have the same expiration date"), *with id.* ("but for the § 154(b) PTA, the '788 Patent would have expired before the '219 Patent"). So it is not clear whether the district court was even considering the right facts.

Finally, in *Mitsubishi*, the challenged patent issued *before* the reference patent (May 17, 2011 vs. July 17, 2012). 2021 WL 1845499, at *27–28. That is opposite the present case where the challenged patent issued *after* the reference patent. Thus, even if we treated a PTA like PTE and double patenting were considered *before* a PTA, the outcome here still would be the opposite of *Mitsubishi* because the challenged patent in *Mitsubishi* was the *earlier* patent whereas the challenged patent here is the *later* patent.

For these reasons, we give little weight to the *Mitsubishi* decision.

Double Patenting Here Was Proper Regardless When the PTA Is Applied

As discussed above, we hold that double patenting should be considered *after* any PTA is applied. Here, after applying the PTA, the challenged patent expired after the reference patent (PTA of 59 days vs. 45 days). Appeal Br. 9 ("the '626 Patent expired 14 days after the '369 Patent" (emphasis omitted)). Thus, the later-expiring claims of the

challenged patent were properly rejected for obviousness-type double patenting over the earlier-expiring claims of the reference patent.

However, even if we treated a PTA like PTE and did a double patenting analysis *before* factoring in any PTA, a double patenting rejection still would be proper here because prior to the PTA, the challenged patent and the reference patent would have expired on the same day (Oct. 6, 2017). *Underwood*, 149 U.S. 224 (affirming a second patent as void when both patents had the same filing date, issue date, and expiration date); *see also* MPEP § 804(I)(B)(1)(b)(ii) ("If both applications are actually filed on the same day, or are entitled to the same earliest effective filing date[,] . . . the provisional nonstatutory double patenting rejection made in each application should be maintained until the rejection is overcome," such as by "filing a terminal disclaimer in the pending application."). Here, the challenged patent is a later-issued patent claiming obvious variants of the earlier-issued reference patent. Even with the same expiration date, double patenting and a terminal disclaimer are still needed to ensure that the later-issued obvious variant retains common ownership with the earlier-issued patent. This is necessary to accomplish double patenting's second goal "to prevent multiple infringement suits by different assignees asserting essentially the same patented invention." *Hubbell*, 709 F.3d at 1145; Ans. 15–16 ("regardless whether two relevant patents have different expiration dates," "the ODP rejection would still be advanced to prevent possible harassment by multiple assignees"); *see also Sandy MacGregor*, 2 F.2d at 657 ("in *Underwood v. Gerber* it was thought that the splitting up of one indivisible right into two and subjecting the infringer to suits by two different owners of the right

infringed justified applying the defense of double patenting as against two patents issued on the same day"); *see also Van Ornum*, 686 F.2d at 945 (similarly summarizing *Underwood*). Appellant never addresses that double patenting applies to patents with the same expiration date.

Appellant does argue that "there has been no harassment by multiple assignees" because the patents have been commonly owned so far and the patents are now expired. Appeal Br. 11. But the statutory time limitation for past damages is "six years prior to the filing of the complaint." 35 U.S.C. § 286. The patents here expired less than six years ago, so the risk still remains for multiple assignees to seek past damages. Indeed, Appellant has already filed one lawsuit after both patents expired. Appeal Br. 2.

Appellant further argues that the patents "will be maintained by the same owner." Appeal Br. 11. The only basis for this assertion is a single paragraph from a declaration of one inventor:

> Because of the exclusive (field-of-use) nature of certain license agreements, MIS/Cellect may not freely assign these patents and they have been, and will continue to be, owned by MIS/Cellect. As the Chief Technology Officer and Co-Founder of Micro Imaging Solutions LLC, I can confirm that MIS/Cellect will not sell off or split apart any portion of the patents that comprise the '626 Patent family to a third-party.

Adair Decl. ¶ 24 (Sept. 8, 2020). But such a declaration is unpersuasive. For example, suppose Appellant went out of business and a bankruptcy court (not Appellant itself) split the patents among various creditors. Even if Appellant's licensees might have a breach-of-contract claim against the new patent owners, a third party sued by the multiple new owners has no way to enforce the inventor's declaration absent double patenting.

There also is no need to wait until *actual* harassment by multiple assignees. *See* Appeal Br. 8 ("this judicially created doctrine requires . . . harassment by multiple assignees"). One goal of double patenting and terminal disclaimers is to preemptively prevent the risk of such harassment:

> Even though both patents are issued to the same patentee or assignee, it (is) possible that ownership of the two will be divided by later transfers and assignments. The possibility of multiple suits against an infringer by assignees of related patents has long been recognized as one of the concerns behind the doctrine of double patenting.

Van Ornum, 686 F.2d at 944 (quoting Chisum on Patents § 9.04(2)(b) (1981)); *see also* Ans. 8.

In sum, the double patenting rejection of the later-issued claims here was proper regardless of whether (A) the PTA is applied before the double patenting analysis (because the challenged patent's post-PTA expiration date is after that of the reference patent) or (B) the PTA is applied after the double patenting analysis (because despite the pre-PTA expiration dates being the same, the challenged patent is a later-issuing obvious variant still at risk for harassment by multiple assignees).

Substantial New Question

Appellant argues there is no substantial new question of patentability because the examiner in the original prosecution was aware of both applications and "conducted an interference search" for both, so the examiner "would have" made a double patenting rejection "if [the examiner] believed that such a rejection was warranted." Appeal Br. 15–17, 10.

We are not persuaded by Appellant's arguments. A substantial new question of patentability does exist here because there is insufficient

evidence that double patenting actually was considered during the original prosecution. Ans. 9–11, 7. Regardless of what ideally should have happened during the original prosecution, the reexamination process exists because items sometimes get overlooked or errors are made. *See, e.g.*, *Patlex Corp. v. Mossinghoff*, 758 F.2d 594, 604 (Fed. Cir. 1985) ("The reexamination statute's purpose is to correct errors made by the government . . . and if need be to remove patents that should never have been granted."), *on reh'g*, 771 F.2d 480, 481 (Fed. Cir. 1985) (denying the petition in relevant part).

Equity

Appellant argues that "an equitable doctrine cannot be applied in a manner that would be inequitable" given that filing a terminal disclaimer "is not possible now" as the patents are expired and "the record is completely devoid" of any "gamesmanship" or "unjustified or improper timewise extension." Appeal Br. 14–15 (quotation omitted).

However, the Federal Circuit is unambiguous that the inequity here is Appellant's enjoyment of a second patent's term beyond the expiration of the first patent:

> When the claims of a patent are obvious in light of the claims of an earlier commonly owned patent, the patentee can have no right to exclude others from practicing the invention encompassed by the later patent after the date of the expiration of the earlier patent. But when a patentee does not terminally disclaim the later patent before the expiration of the earlier related patent, the later patent purports to remain in force even after the date on which the patentee no longer has any right to exclude others from practicing the claimed subject matter. By permitting the later patent to remain in force beyond the date of

> the earlier patent's expiration, the patentee wrongly purports to inform the public that it is precluded from making, using, selling, offering for sale, or importing the claimed invention during a period after the expiration of the earlier patent.
>
> By failing to terminally disclaim a later patent prior to the expiration of an earlier related patent, a patentee enjoys an unjustified advantage—a purported time extension of the right to exclude from the date of the expiration of the earlier patent. The patentee cannot undo this unjustified timewise extension by retroactively disclaiming the term of the later patent because it has *already* enjoyed rights that it seeks to disclaim.

Boehringer, 592 F.3d at 1347–48 (citations omitted); *see also Lonardo*, 119 F.3d at 965. Appellant also never addresses preserving the public's right to make what is covered by the *earlier* patent after it expired:

> The bar against double patenting was created to preserve that bargained-for right held by the public. *See, e.g., Miller v. Eagle Mfg. Co.*, 151 U.S. 186, 197–98, 202 (1894); . . . *Odiorne v. Amesbury Nail Factory*, 18 F.Cas. 578, 579 (C.C.D.Mass.1819). If an inventor could obtain several sequential patents on the same invention, he could retain for himself the exclusive right to exclude or control the public's right to use the patented invention far beyond the term awarded to him under the patent laws. As Justice Story explained in 1819, "[i]t cannot be" that a patentee can obtain two patents in sequence "substantially for the same invention[] and improvements"; "it would completely destroy the whole consideration derived by the public for the grant of the patent, viz. the right to use the invention at the expiration of the term." *Odiorne*, 18 F.Cas. at 579. Thus, the doctrine of double patenting was primarily designed to prevent such harm by limiting a patentee to one patent term per invention or improvement.

Gilead, 753 F.3d at 1212 (parallel citations omitted).

Even beyond the mere existence of the extra term, Appellant concedes that it actively filed at least one lawsuit on the challenged patent after the

expiration of both patents, yet Appellant fails to address whether that lawsuit seeks damages for the extra term of the challenged patent. *See* Appeal Br. 2.

We also agree with the Examiner that invalidating the challenged claims of a *second* patent (or third, fourth, and fifth patents in the case of the numerous related reexaminations here) does not take away Appellant's right to enforce its *first* patent. Ans. 17–18.

Thus, Appellant fails to persuade us that the result here is inequitable.

Conclusion

Appellant argues both double patenting rejections collectively with no separate arguments based on Nguyen. Accordingly, we sustain the double patenting rejections of claims 1, 5, 11, 33, 34, 58, and 64.

OUTCOME

The following table summarizes the outcome of each rejection:

Claim(s) Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1, 5, 11, 33, 34, 58, 64		Double patenting: '369 patent	1, 5, 11, 33, 34, 58, 64	
1, 5, 11, 33, 34, 58, 64		Double patenting: '369 patent and Nguyen	1, 5, 11, 33, 34, 58, 64	
Overall Outcome			1, 5, 11, 33, 34, 58, 64	

TIME TO RESPOND

Requests for extensions of time in this *ex parte* reexamination proceeding are governed by 37 C.F.R. § 1.550(c). *See* 37 C.F.R. § 41.50(f).

AFFIRMED

Appeal 2021-005046
Reexamination Control 90/014,455
Patent 6,452,626 B1

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The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte Cellect LLC
Patent Owner and Appellant

Appeal 2021-005258
Reexamination Control 90/014,457
Patent 7,002,621 B2
Technology Center 3900

Before ALLEN R. MacDONALD, GARTH D. BAER, and MICHAEL J. ENGLE, *Administrative Patent Judges*.

ENGLE, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. §§ 134(b) and 306, Appellant[1] appeals from the rejection of claims 25–29 and 33 of U.S. Patent No. 7,002,621 B2 ("the '621 patent" or "challenged patent") in this *ex parte* reexamination. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

---

[1] Appellant states that the real party in interest is "Cellect LLC, a wholly owned subsidiary of Micro Imaging Solutions LLC." Appeal Br. 2.

TECHNOLOGY

The application relates to "solid state image sensors which are configured to be of a minimum size and used within communication devices specifically including video telephones." '621 patent, 1:21–25.

RELATED MATTERS

The challenged patent and its patent family have been involved in a number of proceedings before federal district courts and the USPTO. Appeal Br. 2 (listing 1 district court case, 20 *inter partes* review petitions, and 5 *ex parte* reexamination requests). Four of the reexaminations involve substantially similar issues on double patenting. *See* Appeal Nos. 2021-005046; 2021-005258; 2021-005302; 2021-005303.

For the challenged patent, two petitions for *inter partes* review were denied institution because the same claims at issue here "all have indiscernible or uncertain scope." IPR2020-00571, Paper 14, at 20 (Oct. 2, 2020); IPR2020-00572, Paper 15, at 20–21 (Oct. 1, 2020). As it was not raised in the present proceeding, we do not address indefiniteness here.

REJECTION

Claims 25–29 and 33 of the '621 patent are rejected for non-statutory double patenting over claims 52, 55, and 61 of U.S. Patent No. 6,452,626 ("the '626 patent" or "reference patent"). Final Act. 4–17.

ISSUE

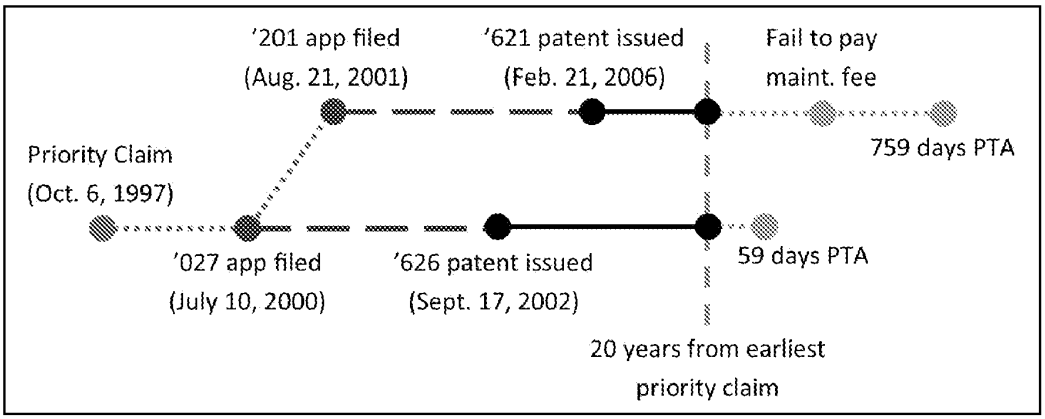
Did the Examiner err in applying an obviousness-type double patenting rejection to two related patents that (1) claim the same priority date, (2) have different patent term adjustments, and (3) are expired?

ANALYSIS

Overview

The challenged patent (the '621 patent) is the child of the reference patent (the '626 patent). The challenged patent issued after the reference patent, but both claim priority to the same application (filed Oct. 6, 1997) so they normally would expire at the same time (Oct. 6, 2017). 35 U.S.C. § 154(a)(2). However, due to various delays by the USPTO during prosecution, both were granted a patent term adjustment ("PTA") under 35 U.S.C. § 154(b), with the challenged patent receiving significantly more PTA than the reference patent (759 days vs. 59 days). Therefore, the reference patent expired *before* the challenged patent. The challenged patent actually expired a few months later—midway through its PTA period—due to Appellant's failure to pay an 11.5-year maintenance fee. Ans. 11. Both patents are now expired, but the statute of limitations for past damages has not yet passed. 35 U.S.C. § 286.

The timeline below shows the relevant dates for the two patents, including priority, filing, issuance, expiration, and PTA, with the challenged patent on top and its parent (the reference patent) below:



Timeline for expiration of '621 patent (top) & '626 patent (bottom)

In this reexamination, the examiners invoked the doctrine of obviousness-type double patenting to reject the claims of the challenged patent as obvious variants of claims in the reference patent. Final Act. 4–17. Appellant does not dispute that the claims of the reference patent would have rendered obvious the claims of the challenged patent. Instead, Appellant argues the reference patent cannot be used for double patenting because (1) a judicially-created doctrine cannot take away statutorily guaranteed time, especially in light of the Federal Circuit's treatment of patent term extensions ("PTE") under 35 U.S.C. § 156, (2) the result would be inequitable given the facts here, and (3) no substantial new question of patentability has been raised because the examiner should have considered double patenting in the original prosecution. *See* Appeal Br. 4–19.

We are not persuaded by Appellant's arguments. First, unlike a PTE under § 156, the statute for a PTA (§ 154) states that any terminal disclaimer should be applied *after* any PTA. Because the primary purpose of a terminal disclaimer is to overcome double patenting, the same rule should apply to double patenting. Moreover, even if double patenting was based on the expiration date *before* applying any PTA (akin to a PTE), double patenting still would be appropriate here because two patents that are obvious variants and expire on the same day still need a terminal disclaimer to enforce common ownership. Second, the result here is not inequitable because the Federal Circuit has said the existence of any extra term of a second patent is itself what is inequitable, and Appellant still enjoyed the entire term of the earliest patent. Third, double patenting is a substantial new question because, regardless of what should have happened in the original

prosecution, there is insufficient evidence that the original examiner actually considered double patenting.

Standard of Review

The PTO is "authorized during reexamination to consider the question of double patenting." *In re Lonardo*, 119 F.3d 960, 966 (Fed. Cir. 1997); *see also* MPEP § 2258(I)(D). "As with statutory obviousness under 35 U.S.C. § 103, obviousness-type double patenting is an issue of law premised on underlying factual inquiries." *Eli Lilly & Co. v. Teva Parenteral Meds., Inc.*, 689 F.3d 1368, 1376 (Fed. Cir. 2012).

Legal Background
on Obviousness-Type Double Patenting, Terminal Disclaimers, PTA, & PTE

Obviousness-type double patenting is a "judicially created" doctrine that "prohibits an inventor from obtaining a second patent for claims that are not patentably distinct from the claims of the first patent." *Lonardo*, 119 F.3d at 965. "There are two justifications for obviousness-type double patenting": (1) "to prevent unjustified timewise extension of the right to exclude granted by a patent no matter how the extension is brought about" and (2) "to prevent multiple infringement suits by different assignees asserting essentially the same patented invention." *In re Hubbell*, 709 F.3d 1140, 1145 (Fed. Cir. 2013) (quotation omitted). For example, if an inventor receives a second patent with claims that are merely obvious variants of a first patent, double patenting helps prevent the patentee from (1) suing on the second patent after the first has already expired (i.e., improper time-wise extension) or (2) selling the two patents to different entities only to have

both entities separately sue an alleged infringer on two obvious variants of each other (i.e., improper harassment by multiple assignees).

A patentee or applicant often can overcome double patenting by filing a terminal disclaimer. *Boehringer Ingelheim Int'l GmbH v. Barr Labs., Inc.*, 592 F.3d 1340, 1346 (Fed. Cir. 2010). Terminal disclaimers are expressly permitted by statute to "disclaim or dedicate to the public . . . any terminal part of the term" of a patent. 35 U.S.C. § 253(b). The USPTO has provided regulations on what a terminal disclaimer must contain to be effective. *E.g.*, 37 C.F.R. § 1.321. A terminal disclaimer solves the two concerns of double patenting by (1) making the *later* patent expire with the *earlier* patent and (2) rendering the second patent unenforceable if it is not commonly owned with the first patent. *E.g.*, 37 C.F.R. § 1.321(b)(2), (c)(3), (d)(3); MPEP §§ 804.02(VI), 1490(VI)(A), (IX). However, "a terminal disclaimer filed after the expiration of the earlier patent over which claims have been found obvious cannot cure obviousness-type double patenting." *Boehringer*, 592 F.3d at 1347–48. Thus, a terminal disclaimer cannot cure any double patenting rejection against the expired patents here. Appeal Br. 17–18.

For two issued patents, double patenting and the need for a terminal disclaimer generally only apply to the *later* patent.[2] *See Eli Lilly & Co. v. Barr Labs., Inc.*, 251 F.3d 955, 968 & n.5 (Fed. Cir. 2001) ("A *later* claim that is not patentably distinct from an earlier claim in a commonly owned patent is invalid for obvious-type double patenting."; "A patent owner cannot avoid double patenting by disclaiming the *earlier* patent." (emphases

[2] For two co-pending applications, a provisional double patenting rejection against both applications may be appropriate if it is not yet known which will result in the later patent. *See* MPEP § 804(I)(1).

added)). The question then is how to determine which patent is "later." The answer depends on whether the patents issued from applications filed on or after June 8, 1995. This date is six months after enactment of the Uruguay Round Agreements Act ("URAA"), which changed the term of a patent from (A) 17 years after issue to (B) 20 years from the earliest filing date of any non-provisional U.S. application to which that patent claims priority. 35 U.S.C. § 154.

For two post-URAA patents, the "later" patent generally is determined by looking at the *expiration* date. *Novartis Pharms. Corp. v. Breckenridge Pharm. Inc.*, 909 F.3d 1355, 1362–63, 1366 (Fed. Cir. 2018). For two pre-URAA patents or certain scenarios involving one patent on each side of the URAA date, the "later" patent is instead determined by looking at the *issue* date. *Id.* at 1362 ("Traditionally, courts looked at the issuance dates of the respective patents, because, under the law pre-URAA, the expiration date of the patent was inextricably intertwined with the issuance date, and used the earlier-issued patent to limit the patent term(s) of the later issued patent(s)."). Prior to the URAA, a patent expired 17 years after issuance, so "looking to patent issue dates had previously served as a reliable stand-in for the date that really mattered—patent expiration." *Gilead Scis., Inc. v. Natco Pharma Ltd.*, 753 F.3d 1208, 1215 (Fed. Cir. 2014). Finally, if two post-URAA patents expire on the same day or two pre-URAA patents have the same issue date, then the patent with the higher patent number may be invalid for double patenting.[3] *See Underwood v. Gerber*, 149 U.S. 224

[3] As the patents here issued on different dates, we need not resolve whether an analysis for patents issued on the same day should first look to priority date or filing date rather than patent number (e.g., two pre-URAA patents

(1893) (affirming Patent No. 348,073 was void over the same inventors' Patent No. 348,072 when both patents had the same filing date, issue date, and expiration date).

A complication arises, however, in that Congress also provided two ways to potentially prolong the term of a patent. A patent term adjustment ("PTA") under § 154(b) may adjust the term based on certain delays by the USPTO during prosecution, and a patent term extension ("PTE") under § 156 may extend the term based on certain regulatory delays, such as the FDA reviewing a new drug. 35 U.S.C. §§ 154(b), 156. The question before us now is how a PTA under § 154 should factor into the double patenting analysis, such as whether double patenting should be based on the expiration date *before* a PTA or *after*. The Federal Circuit already addressed similar questions for a PTE, yet it did so by contrasting the statutes for PTE (§ 156) versus PTA (§ 154). We discuss these cases below.

PTE & Terminal Disclaimers
(Merck v. Hi-Tech)

For a PTE under § 156, the starting point is *Merck & Co. v. Hi-Tech Pharmacal Co.*, 482 F.3d 1317 (Fed. Cir. 2007). In that case, the patent owner had already filed a terminal disclaimer to overcome an obviousness-type double patenting rejection. 482 F.3d at 1318–19. Later, the patent was awarded a PTE under § 156. *Id.* at 1319. The question before the court was whether a PTE under § 156 could be applied to a patent subject to a terminal disclaimer. *Id.* at 1324. The court held "a patent term extension under § 156

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with the same issue date but the patent with the higher patent number has a significantly earlier filing date and priority date).

is not foreclosed by a terminal disclaimer." *Id.* at 1322. In particular, "[t]he computation of a Hatch–Waxman patent term extension is from the expiration date resulting from the terminal disclaimer and not from the date the patent would have expired in the absence of the terminal disclaimer." *Id.* at 1322–23. Put another way, a PTE under § 156 is applied *after* any terminal disclaimer.

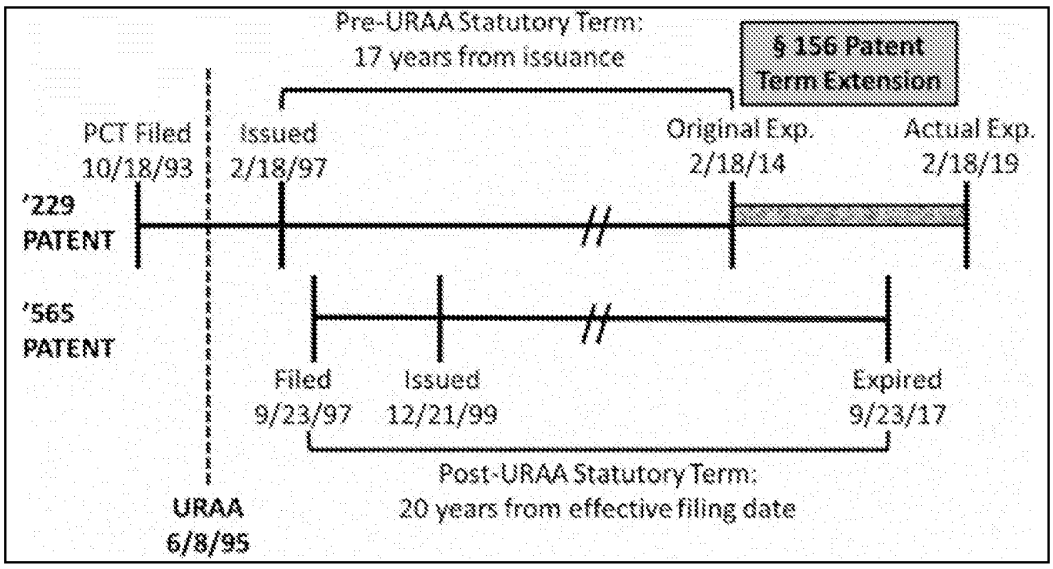
The Federal Circuit reached this conclusion by contrasting PTE with PTA. For a PTA, "§ 154(b)(2)(B) expressly excludes patents in which a terminal disclaimer was filed from the benefit of a term adjustment for PTO delays." *Merck v. Hi-Tech*, 482 F.3d at 1322. Specifically, the statute states that "[n]o patent the term of which has been disclaimed beyond a specified date may be adjusted under this section beyond the expiration date specified in the disclaimer." 35 U.S.C. § 154(b)(2)(B). The Federal Circuit explained that "[t]here is no similar provision that excludes patents in which a terminal disclaimer was filed from the benefits of Hatch-Waxman extensions" under § 156. *Merck v. Hi-Tech*, 482 F.3d at 1322. Thus, a terminal disclaimer is applied *before* a PTE *because* PTE is different than PTA.

PTE & Double Patenting
(Novartis v. Ezra)

The next question was how a PTE applied to double patenting in the absence of a terminal disclaimer. As noted above, a terminal disclaimer generally is filed to overcome obviousness-type double patenting. *In re Van Ornum*, 686 F.2d 937, 948 (CCPA 1982); 37 C.F.R. § 1.321(c), (d); MPEP § 1490(II). Given this relationship between double patenting and terminal disclaimers and given the holding in *Merck v. Hi-Tech* that a terminal disclaimer applies *before* a PTE, the Federal Circuit not surprisingly held "as

a logical extension of our holding in *Merck & Co. v. Hi-Tech*" that double patenting also should be considered *before* a PTE. *Novartis AG v. Ezra Ventures LLC*, 909 F.3d 1367, 1373–74 (Fed. Cir. 2018). Thus, "if a patent, under its original expiration date without a PTE, should have been (but was not) terminally disclaimed because of obviousness-type double patenting, then this court's obviousness-type double patenting case law would apply, and the patent could be invalidated." *Id.* at 1374. "However, if a patent, under its pre-PTE expiration date, is valid under all other provisions of law, then it is entitled to the full term of its PTE." *Id.*

A timeline for the patents in *Novartis v. Ezra* is reproduced below:



Novartis v. Ezra, 909 F.3d at 1370. As shown in the timeline above, the challenged patent (the '229 patent) had an *earlier* filing date, issue date, and pre-PTE expiration date than the reference patent (the '565 patent). Because the challenged patent was the *earlier* patent (at least pre-PTE), the challenged patent was not invalid for double patenting. *Id.* at 1373–75.

PTA & Double Patenting

The question now before us is how a PTA affects double patenting. Appellant relies on one broadly worded sentence in *Novartis v. Ezra* to argue that "a judge-made doctrine" (i.e., obviousness-type double patenting) cannot "cut off a statutorily-authorized time extension." Appeal Br. 10 (quoting *Novartis v. Ezra*, 909 F.3d at 1375). Although the holding in *Novartis v. Ezra* was about a PTE under § 156, Appellant extends that argument to suggest that any PTA under § 154 also is a "statutory grant of additional term" that "cannot be deemed improper." *Id.*

Appellant's argument is not persuasive because it ignores the plain text of § 154 and the actual holding in *Novartis v. Ezra*.

First, contrary to Appellant's assertions, the decision in *Novartis v. Ezra* reaffirms that a double patenting analysis *should* be done even if a patent has a PTE. The real question was whether double patenting should be considered *before* or *after* a PTE, with the court ultimately deciding double patenting should be considered *before* a PTE. *Novartis v. Ezra*, 909 F.3d at 1374 ("if a patent, under its original expiration date without a PTE, should have been (but was not) terminally disclaimed because of obviousness-type double patenting, then this court's obviousness-type double patenting case law would apply, and the patent could be invalidated"). So here, we must do a double patenting analysis and the question is whether double patenting should be considered with the expiration dates *before* or *after* a PTA.

Second, the outcome for a PTE under § 156 in *Merck v. Hi-Tech* was based on the difference between § 156 and § 154. In particular, "§ 154(b)(2)(B) expressly excludes patents in which a terminal disclaimer was filed from the benefit of a term adjustment for PTO delays," but there is

an "absence of any such prohibition regarding Hatch–Waxman extensions" under § 156. *Merck v. Hi-Tech*, 482 F.3d at 1322. That reasoning in *Merck v. Hi-Tech* was important enough that when summarizing the prior case, *Novartis v. Ezra* repeated the prior case's "contrast between § 156 for PTE with the language of § 154 for patent term adjustments." *Novartis v. Ezra*, 909 F.3d at 1373–74. Thus, the rule in *Merck v. Hi-Tech* and *Novartis v. Ezra* for when to apply a PTE does not apply to a PTA because those decisions were premised on the contrast between PTE and PTA.

Third, the statutory language in § 154 is clear that any terminal disclaimer should be applied *after* any PTA (i.e., a PTA cannot adjust a term beyond the expiration date in any disclaimer). 35 U.S.C. § 154(b)(2)(B) ("No patent the term of which has been disclaimed beyond a specified date may be adjusted under this section beyond the expiration date specified in the disclaimer."). Although Appellant asserts that the statute says the term "shall" be extended (Reply Br. 8), Appellant omits that all of those sentences are prefaced with the phrase "Subject to the limitations under paragraph (2)," which includes the limitations due to terminal disclaimers. *Id.* § 154(b)(1)(A), (B), (C). Thus, as recognized by *Merck v. Hi-Tech* and *Novartis v. Ezra*, the statute itself is clear that unlike a PTE under § 156, a PTA under § 154 shall *not* extend the term of a patent past the date of any terminal disclaimer.

Fourth, given that terminal disclaimers arise almost exclusively to overcome obviousness-type double patenting, Congress expressly addressing terminal disclaimers in § 154 is tantamount to addressing obviousness-type double patenting. *See Van Ornum*, 686 F.2d at 948; 37 C.F.R. § 1.321(c), (d); MPEP § 1490(II). Indeed, *Novartis v. Ezra* itself recognized that a rule

for terminal disclaimers (from *Merck v. Hi-Tech*) should also apply to obviousness-type double patenting as "a logical extension." 909 F.3d at 1373. The *Novartis v. Ezra* court rejected the argument "that the *Merck* court's rationale only spoke to the impact of a new PTE on preexisting terminal disclaimers," instead finding that the prior "holding on the validity of a PTE for a patent that was terminally disclaimed *in order to overcome an obviousness-type double patenting rejection* is directly relevant to the instant case." *Id.* at 1374 (quotation omitted). Obviousness-type double patenting and terminal disclaimers are two sides of the same coin: the problem and the solution. Just as *Novartis v. Ezra* found a rule on terminal disclaimers was "directly relevant" to double patenting and therefore applied that rule to double patenting as "a logical extension," so too we hold that the statutory rule for terminal disclaimers in § 154 is directly relevant to double patenting and we apply that same rule to double patenting as a logical extension.

Indeed, in at least one related reexamination, Appellant itself argues that double patenting should be applied to post-PTA dates. *Compare* Appeal 2021-005302, Appeal Br. 7 ("the '369 Patent . . . and '626 Patent . . . have the same expiration date except for statutorily-authorized PTA"), *with id.* at 10 n.1 ("the '626 Patent cannot be used as an obviousness-type double patenting reference because the '626 Patent expired after the '369 Patent").

Finally, the Federal Circuit also previously said that "another crucial purpose of the doctrine" of double patenting was "to prevent an inventor from securing a second, later expiring patent" for "[p]atents . . . filed at the same time" that "have different patent terms due to examination delays at the PTO" under "§ 154(b) (patent term adjustments)." *AbbVie Inc. v. Mathilda & Terence Kennedy Inst. of Rheumatology Tr.*, 764 F.3d 1366,

1373 (Fed. Cir. 2014); *see also In re Fallaux*, 564 F.3d 1313, 1319 (Fed. Cir. 2009) ("In some cases there may still be the possibility of an unjust time-wise extension of a patent arising from patent term adjustment under § 154 or patent term extension under § 156."). That is precisely the scenario we have here where two patents have the same effective filing date but expire at different times due solely to PTAs.

Appellant provides no plausible reason for ignoring the clear statutory text and the contrast between § 154 and § 156 that formed the basis of *Merck v. Hi-Tech* and *Novartis v. Ezra*. Nor has Appellant provided any reason for applying the *post*-PTA date for terminal disclaimers yet the *pre*-PTA date for double patenting.[4] We therefore hold that both obviousness-type double patenting and terminal disclaimers should be considered *after* any PTA.[5]

The District Court Decision in Mitsubishi Is Not Persuasive

Appellant also cites a district court decision in *Mitsubishi Tanabe Pharma Corp. v. Sandoz, Inc.*, No. 3:17-cv-05319, __ F. Supp. 3d __, 2021

[4] Applying different dates for double patenting versus terminal disclaimers also creates inconsistent results. For example, suppose the pre-PTA expiration date of Patent A is 1 day after Patent B. Therefore, Patent B could be used as a double patenting reference (pre-PTA) against Patent A, and a terminal disclaimer (post-PTA) would wipe out *all* PTA on Patent A. However, Patent A could *not* be used as a double patenting reference (pre-PTA) against Patent B, so Patent B could have an unlimited amount of PTA, even long after the expiration of Patent A.

[5] 35 U.S.C. § 154(b)(3)(A) gives the Director some discretion "establishing procedures for the application for and determination of patent term adjustments." Because we decide the case based on the reasoning above, we need not decide whether that discretion includes the PTA issues here.

WL 1845499, at *27–30 (D.N.J. Mar. 22, 2021). Appeal Br. 13–17. We do not find Appellant's citation to *Mitsubishi* persuasive. *See also* Ans. 10.

First, an earlier district court decision in the Western District of Michigan came out the opposite way from *Mitsubishi*. *Magna Elecs., Inc. v. TRW Automotive Holdings Corp.*, No. 12-cv-654, 2015 WL 11430786 (W.D. Mich. Dec. 10, 2015). Although the *Magna Electronics* case appears to have settled prior to any appeal, we understand that the decision in *Mitsubishi* is currently on appeal to the Federal Circuit (No. 21-1876; filed Apr 23, 2021).

Second, the *Mitsubishi* district court never addressed that double patenting applies even to two patents that have the same filing date, the same issue date, and the same expiration date. *Underwood*, 149 U.S. 224. For example, a terminal disclaimer is still needed to ensure that two patents remain commonly owned. *See Sandy MacGregor Co. v. Vaco Grip Co.*, 2 F.2d 655, 657 (6th Cir. 1924) ("in *Underwood v. Gerber* it was thought that the splitting up of one indivisible right into two and subjecting the infringer to suits by two different owners of the right infringed justified applying the defense of double patenting as against two patents issued on the same day"); *Van Ornum*, 686 F.2d at 945 (similarly summarizing *Underwood*).

Third, the district court's entire discussion of the difference between § 154 and § 156 is relegated to a single footnote in which the court does not appear to have understood that a terminal disclaimer is the standard way to cure double patenting, thereby overlooking why the Federal Circuit decided a rule for terminal disclaimers (*Merck v. Hi-Tech*) should also apply to a double patenting analysis (*Novartis v. Ezra*) as a "logical extension." *See Mitsubishi*, 2021 WL 1845499, at *29 n.45.

Fourth, even within the same paragraph, the district court confuses when the challenged patent would have expired relative to the reference patent. *Compare Mitsubishi*, 2021 WL 1845499, at *29 ("absent the PTA granted to the '788 Patent, both the '788 Patent and the '219 Patent would have the same expiration date"), *with id.* ("but for the § 154(b) PTA, the '788 Patent would have expired before the '219 Patent"). So it is not clear whether the district court was even considering the right facts.

Finally, in *Mitsubishi*, the challenged patent issued *before* the reference patent (May 17, 2011 vs. July 17, 2012). 2021 WL 1845499, at *27–28. That is opposite the present case where the challenged patent issued *after* the reference patent. Thus, even if we treated a PTA like PTE and double patenting were considered *before* a PTA, the outcome here still would be the opposite of *Mitsubishi* because the challenged patent in *Mitsubishi* was the *earlier* patent whereas the challenged patent here is the *later* patent.

For these reasons, we give little weight to the *Mitsubishi* decision.

Double Patenting Here Was Proper Regardless When the PTA Is Applied

As discussed above, we hold that double patenting should be considered *after* any PTA is applied. Here, after applying the PTA, the challenged patent expired after the reference patent (PTA of 759 days vs. 59 days). Appeal Br. 8–9. Even factoring in the actual expiration date from Appellant's failure to pay the maintenance fee, "the '621 Patent expired . . . 80 days after the '626 expired." *Id.* at 9 (emphasis omitted). Thus, the later-expiring claims of the challenged patent were properly rejected for

obviousness-type double patenting over the earlier-expiring claims of the reference patent.

However, even if we treated a PTA like PTE and did a double patenting analysis *before* factoring in any PTA, a double patenting rejection still would be proper here because prior to the PTA, the challenged patent and the reference patent would have expired on the same day (Oct. 6, 2017). *Underwood*, 149 U.S. 224 (affirming a second patent as void when both patents had the same filing date, issue date, and expiration date); *see also* MPEP § 804(I)(B)(1)(b)(ii) ("If both applications are actually filed on the same day, or are entitled to the same earliest effective filing date[,] . . . the provisional nonstatutory double patenting rejection made in each application should be maintained until the rejection is overcome," such as by "filing a terminal disclaimer in the pending application."). Here, the challenged patent is a later-issued patent claiming obvious variants of the earlier-issued reference patent. Even with the same expiration date, double patenting and a terminal disclaimer are still needed to ensure that the later-issued obvious variant retains common ownership with the earlier-issued patent. This is necessary to accomplish double patenting's second goal "to prevent multiple infringement suits by different assignees asserting essentially the same patented invention." *Hubbell*, 709 F.3d at 1145; *see also Sandy MacGregor*, 2 F.2d at 657 ("in *Underwood v. Gerber* it was thought that the splitting up of one indivisible right into two and subjecting the infringer to suits by two different owners of the right infringed justified applying the defense of double patenting as against two patents issued on the same day"); *see also Van Ornum*, 686 F.2d at 945 (similarly summarizing *Underwood*).

Appellant never addresses that double patenting applies to patents with the same expiration date.

Appellant does argue that "there has been no harassment by multiple assignees" because the patents have been commonly owned so far and the patents are now expired. Appeal Br. 10. But the statutory time limitation for past damages is "six years prior to the filing of the complaint." 35 U.S.C. § 286. The patents here expired less than six years ago, so the risk still remains for multiple assignees to seek past damages. Indeed, Appellant has already filed one lawsuit after both patents expired. Appeal Br. 2.

Appellant further argues that the patents "will be maintained by the same owner." Appeal Br. 10. The only basis for this assertion is a single paragraph from a declaration of one inventor:

> Because of the exclusive (field-of-use) nature of certain license agreements, MIS/Cellect may not freely assign these patents and they have been, and will continue to be, owned by MIS/Cellect. As the Chief Technology Officer and Co-Founder of Micro Imaging Solutions LLC, I can confirm that MIS/Cellect will not sell off or split apart any portion of the patents that comprise the '621 Patent family to a third-party.

Adair Decl. ¶ 24. But such a declaration is unpersuasive. For example, suppose Appellant went out of business and a bankruptcy court (not Appellant itself) split the patents among various creditors. Even if Appellant's licensees might have a breach-of-contract claim against the new patent owners, a third party sued by the multiple new owners has no way to enforce the inventor's declaration absent double patenting.

There also is no need to wait until *actual* harassment by multiple assignees. *See* Appeal Br. 7 ("this judicially created doctrine requires . . .

harassment by multiple assignees"). One goal of double patenting and terminal disclaimers is to preemptively prevent the risk of such harassment:

> Even though both patents are issued to the same patentee or assignee, it (is) possible that ownership of the two will be divided by later transfers and assignments. The possibility of multiple suits against an infringer by assignees of related patents has long been recognized as one of the concerns behind the doctrine of double patenting.

Van Ornum, 686 F.2d at 944 (quoting Chisum on Patents § 9.04(2)(b) (1981)).

In sum, the double patenting rejection of the later-issued claims here was proper regardless of whether (A) the PTA is applied before the double patenting analysis (because the challenged patent's post-PTA expiration date is after that of the reference patent) or (B) the PTA is applied after the double patenting analysis (because despite the pre-PTA expiration dates being the same, the challenged patent is a later-issuing obvious variant still at risk for harassment by multiple assignees).

Substantial New Question

Appellant argues there is no substantial new question of patentability because the examiner in the original prosecution was aware of both applications and "conducted an interference search" for both, so the examiner "would have" made a double patenting rejection "if [the examiner] believed that such a rejection was warranted." Appeal Br. 18–19, 9.

We are not persuaded by Appellant's arguments. A substantial new question of patentability does exist here because there is insufficient evidence that double patenting actually was considered during the original prosecution. Ans. 12, 5. Regardless of what ideally should have happened

during the original prosecution, the reexamination process exists because items sometimes get overlooked or errors are made. *See, e.g.*, *Patlex Corp. v. Mossinghoff*, 758 F.2d 594, 604 (Fed. Cir. 1985) ("The reexamination statute's purpose is to correct errors made by the government . . . and if need be to remove patents that should never have been granted."), *on reh'g*, 771 F.2d 480, 481 (Fed. Cir. 1985) (denying the petition in relevant part).

Equity

Appellant argues that "an equitable doctrine should not be applied in a manner that would be inequitable" given that "filing a terminal disclaimer now is not possible as the patents are expired" and "the record is completely devoid" of any "gamesmanship" or "unjustified or improper timewise extension." Appeal Br. 17–18 (quotation omitted). According to Appellant, "the '621 and '626 Patents have different claim scopes, and thus are different property rights, so Patent Owner is separately entitled to them." Reply Br. 10.

However, the Federal Circuit is unambiguous that the inequity here is Appellant's enjoyment of a second patent's term beyond the expiration of the first patent:

> When the claims of a patent are obvious in light of the claims of an earlier commonly owned patent, the patentee can have no right to exclude others from practicing the invention encompassed by the later patent after the date of the expiration of the earlier patent. But when a patentee does not terminally disclaim the later patent before the expiration of the earlier related patent, the later patent purports to remain in force even after the date on which the patentee no longer has any right to exclude others from practicing the claimed subject matter. By permitting the later patent to remain in force beyond the date of the earlier patent's expiration, the patentee wrongly purports to

> inform the public that it is precluded from making, using, selling, offering for sale, or importing the claimed invention during a period after the expiration of the earlier patent.
>
> By failing to terminally disclaim a later patent prior to the expiration of an earlier related patent, a patentee enjoys an unjustified advantage—a purported time extension of the right to exclude from the date of the expiration of the earlier patent. The patentee cannot undo this unjustified timewise extension by retroactively disclaiming the term of the later patent because it has *already* enjoyed rights that it seeks to disclaim.

Boehringer, 592 F.3d at 1347–48 (citations omitted); *see also Lonardo*, 119 F.3d at 965. Appellant also never addresses preserving the public's right to make what is covered by the *earlier* patent after it expired:

> The bar against double patenting was created to preserve that bargained-for right held by the public. *See, e.g., Miller v. Eagle Mfg. Co.*, 151 U.S. 186, 197–98, 202 (1894); . . . *Odiorne v. Amesbury Nail Factory*, 18 F.Cas. 578, 579 (C.C.D.Mass.1819). If an inventor could obtain several sequential patents on the same invention, he could retain for himself the exclusive right to exclude or control the public's right to use the patented invention far beyond the term awarded to him under the patent laws. As Justice Story explained in 1819, "[i]t cannot be" that a patentee can obtain two patents in sequence "substantially for the same invention[] and improvements"; "it would completely destroy the whole consideration derived by the public for the grant of the patent, viz. the right to use the invention at the expiration of the term." *Odiorne*, 18 F.Cas. at 579. Thus, the doctrine of double patenting was primarily designed to prevent such harm by limiting a patentee to one patent term per invention or improvement.

Gilead, 753 F.3d at 1212 (parallel citations omitted).

Even beyond the mere existence of the extra term, Appellant concedes that it actively filed at least one lawsuit on the challenged patent after the

expiration of both patents, yet Appellant fails to address whether that lawsuit seeks damages for the extra term of the challenged patent. *See* Appeal Br. 2.

We also agree with the Examiner that invalidating the challenged claims of a *second* patent (or third, fourth, and fifth patents in the case of the numerous related reexaminations here) does not take away Appellant's right to enforce its *first* patent. Ans. 11.

Thus, Appellant fails to persuade us that the result here is inequitable.

Conclusion

Accordingly, we sustain the double patenting rejection of claims 25–29 and 33.

OUTCOME

The following table summarizes the outcome of the rejection:

Claim(s) Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
25–29, 33		Obviousness-Type Double Patenting: '626 patent	25–29, 33	

TIME TO RESPOND

Requests for extensions of time in this *ex parte* reexamination proceeding are governed by 37 C.F.R. § 1.550(c). *See* 37 C.F.R. § 41.50(f).

AFFIRMED

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US006982742B2

(12) **United States Patent**
Adair et al.

(10) **Patent No.: US 6,982,742 B2**
(45) **Date of Patent: Jan. 3, 2006**

(54) **HAND-HELD COMPUTERS INCORPORATING REDUCED AREA IMAGING DEVICES**

(76) Inventors: **Edwin L. Adair**, 317 Paragon Way, Castle Pines Village, CO (US) 80104; **Jeffrey L. Adair**, 1861 E. Redfox Pl., Highlands Ranch, CO (US) 80126; **Randall S. Adair**, 3082 S. Flamingo Way, Denver, CO (US) 80222

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 726 days.

(21) Appl. No.: **09/935,993**

(22) Filed: **Aug. 23, 2001**

(65) **Prior Publication Data**

US 2002/0067408 A1 Jun. 6, 2002

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/638,976, filed on Aug. 15, 2000, now Pat. No. 6,424,369, which is a continuation-in-part of application No. 09/496,312, filed on Feb. 1, 2000, now Pat. No. 6,275,255, which is a continuation of application No. 09/175,685, filed on Oct. 20, 1998, now Pat. No. 6,043,839, which is a continuation-in-part of application No. 08/944,322, filed on Oct. 6, 1997, now Pat. No. 5,929,901.

(51) **Int. Cl.**
H04Q 7/32 (2006.01)

(52) **U.S. Cl.** **348/158**; 455/556

(58) **Field of Classification Search** 348/65–76, 348/143–160, 373–376; 455/556–570; 382/310–320; 345/327, 351
See application file for complete search history.

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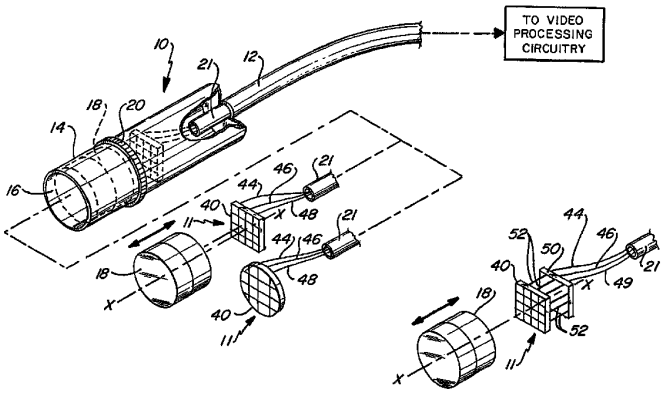
Primary Examiner—Andy Rao
(74) *Attorney, Agent, or Firm*—Sheridan Ross PC

(57) **ABSTRACT**

A reduced area-imaging device is provided for use with a miniature hand-held computer referred to in the industry as a PDA. Various configurations of the imaging device are provided which position elements of the imaging device in desired locations. The PDA includes a miniature LCD-type video screen which can display not only images taken by the camera module, but also incoming video images. The camera module may communicate with the housing of the PDA either by a wired connection, or wirelessly. The camera module is small enough that it can be stored within the housing of the PDA. The camera module may be pointed at an object within sight of the user without having to move the PDA housing in order to take an image. Any acceptable wireless standard may be used for wireless communication between the camera module and the PDA. One particularly advantageous standard includes Bluetooth.

83 Claims, 14 Drawing Sheets



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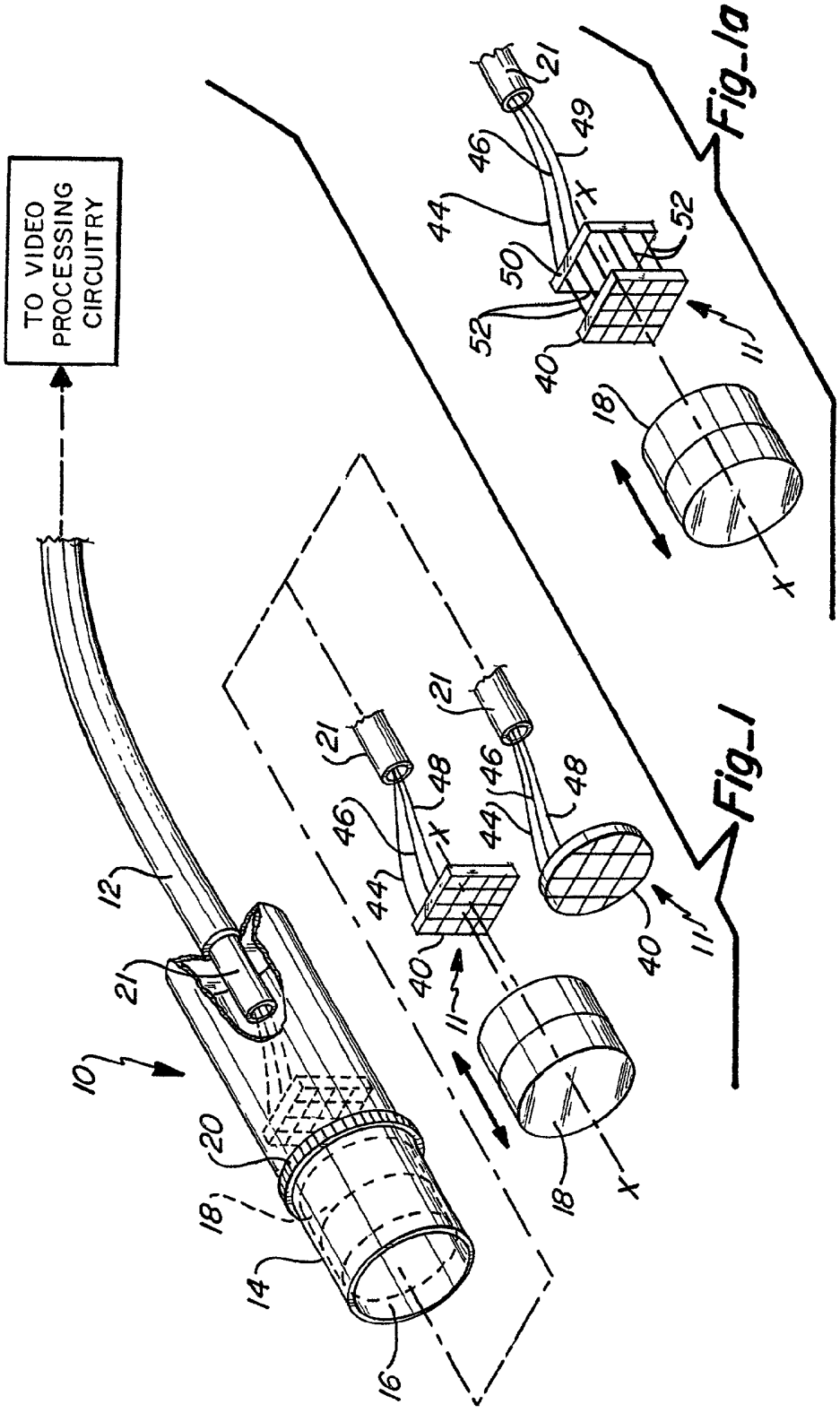

TO VIDEO PROCESSING CIRCUITRY
10
12
14
16
18
20
21
40
44
46
48
49
50
52
X
111

Fig_1a

Fig_1

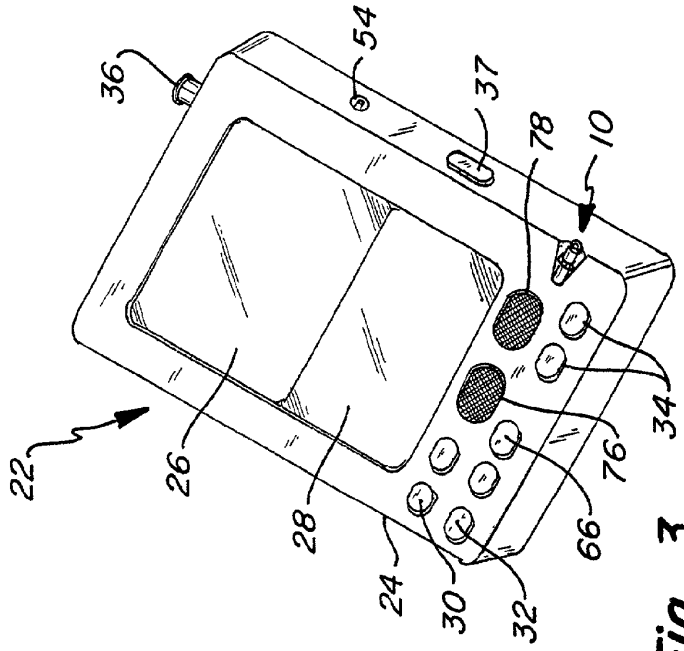

36
54
37
78
10
22
26
28
24
30
32
66
76
34

Fig-3

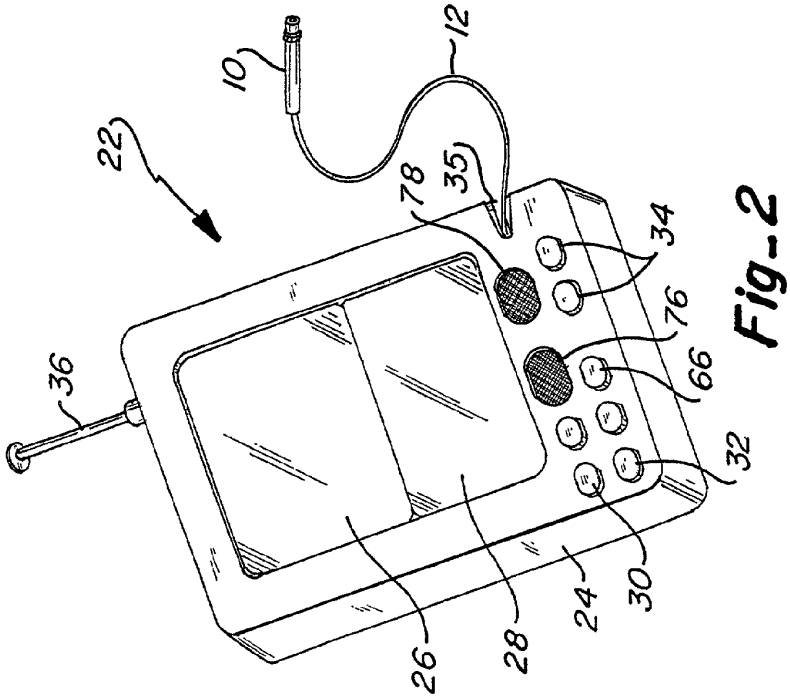

10
12
22
78
35
34
76
66
36
32
26
28
24
30

Fig-2

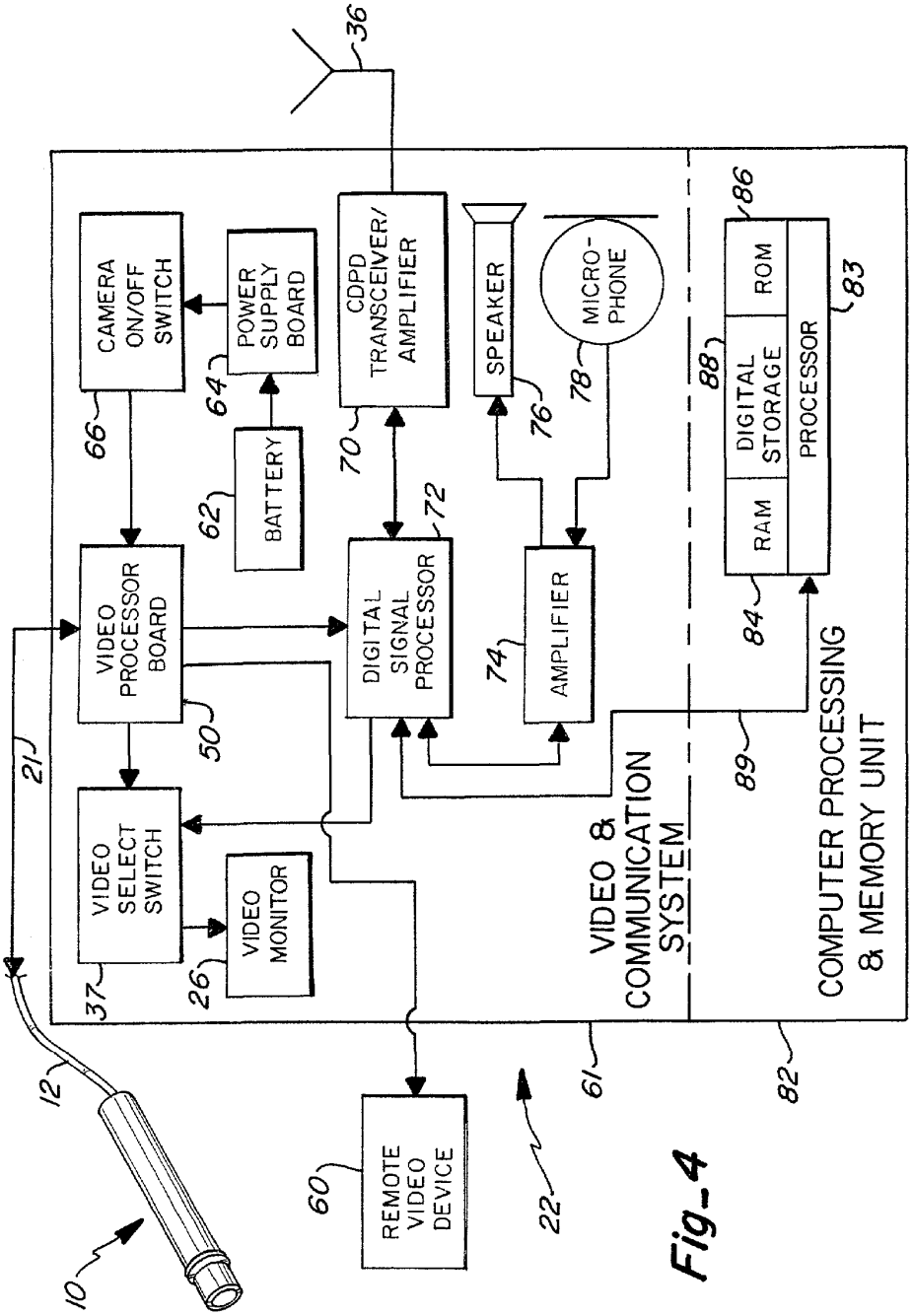

36
CAMERA ON/OFF SWITCH
POWER SUPPLY BOARD
CDPD TRANSCEIVER/ AMPLIFIER
SPEAKER
MICRO-PHONE
ROM
DIGITAL STORAGE
PROCESSOR
RAM
BATTERY
VIDEO PROCESSOR BOARD
DIGITAL SIGNAL PROCESSOR
AMPLIFIER
VIDEO SELECT SWITCH
VIDEO MONITOR
REMOTE VIDEO DEVICE
VIDEO & COMMUNICATION SYSTEM
COMPUTER PROCESSING & MEMORY UNIT
10
12
21
22
26
37
50
60
61
62
64
66
70
72
74
76
78
82
83
84
86
88
89

Fig_4

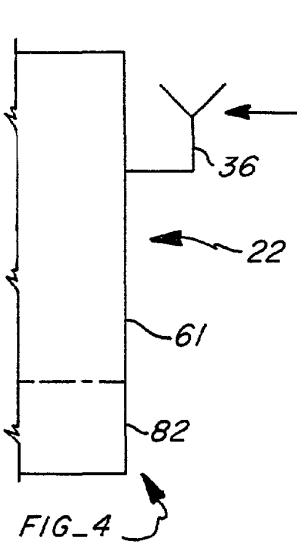


FIG_4

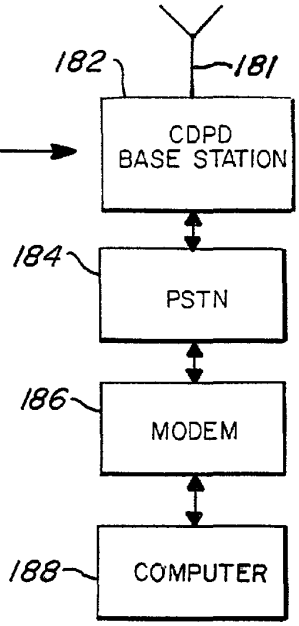


Fig_5

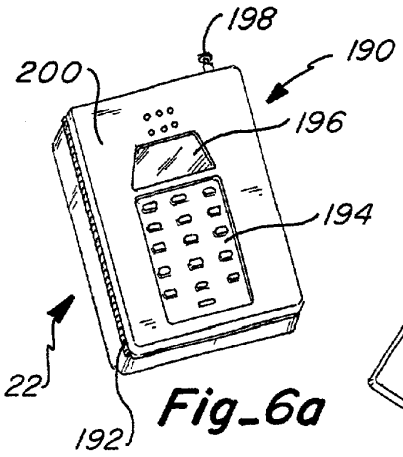


Fig_6a

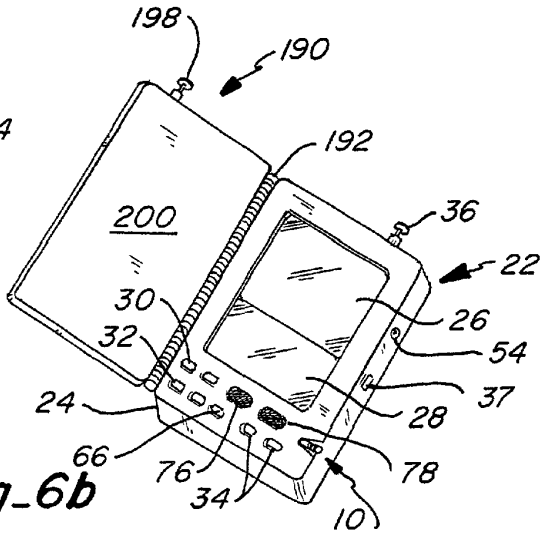


Fig_6b

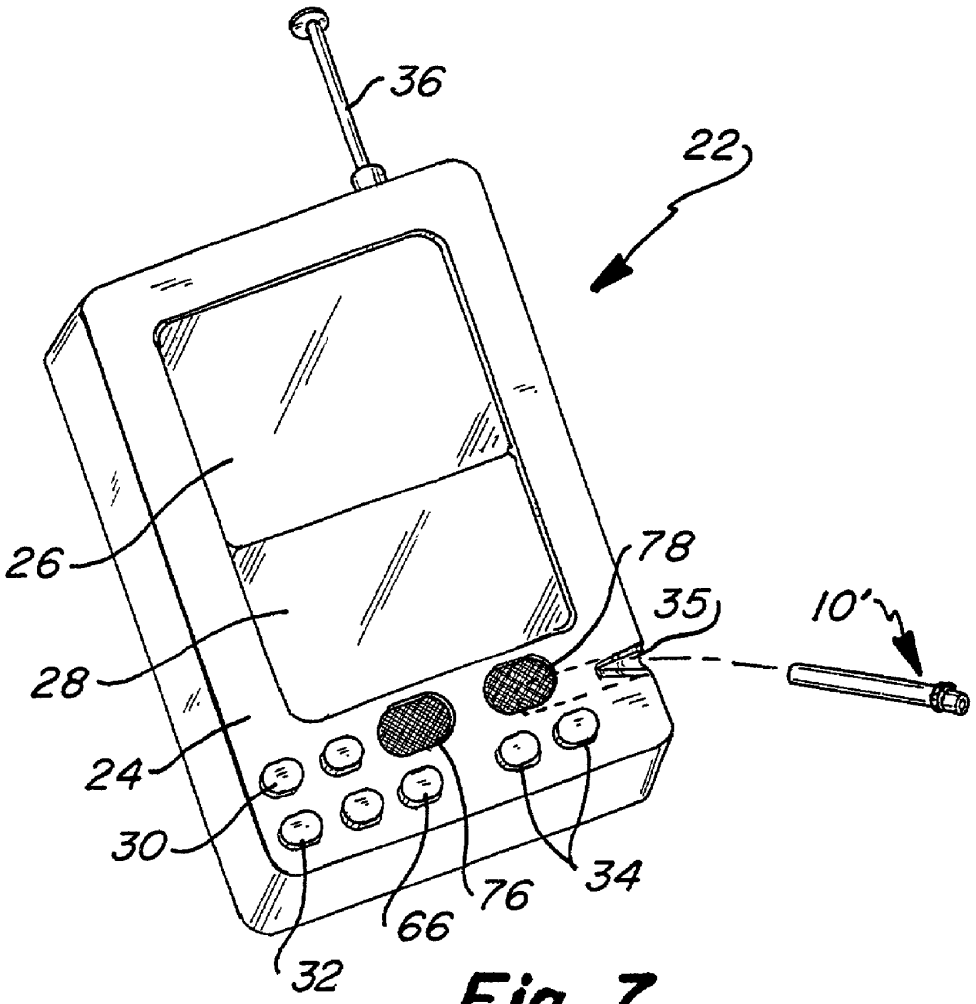


Fig_7

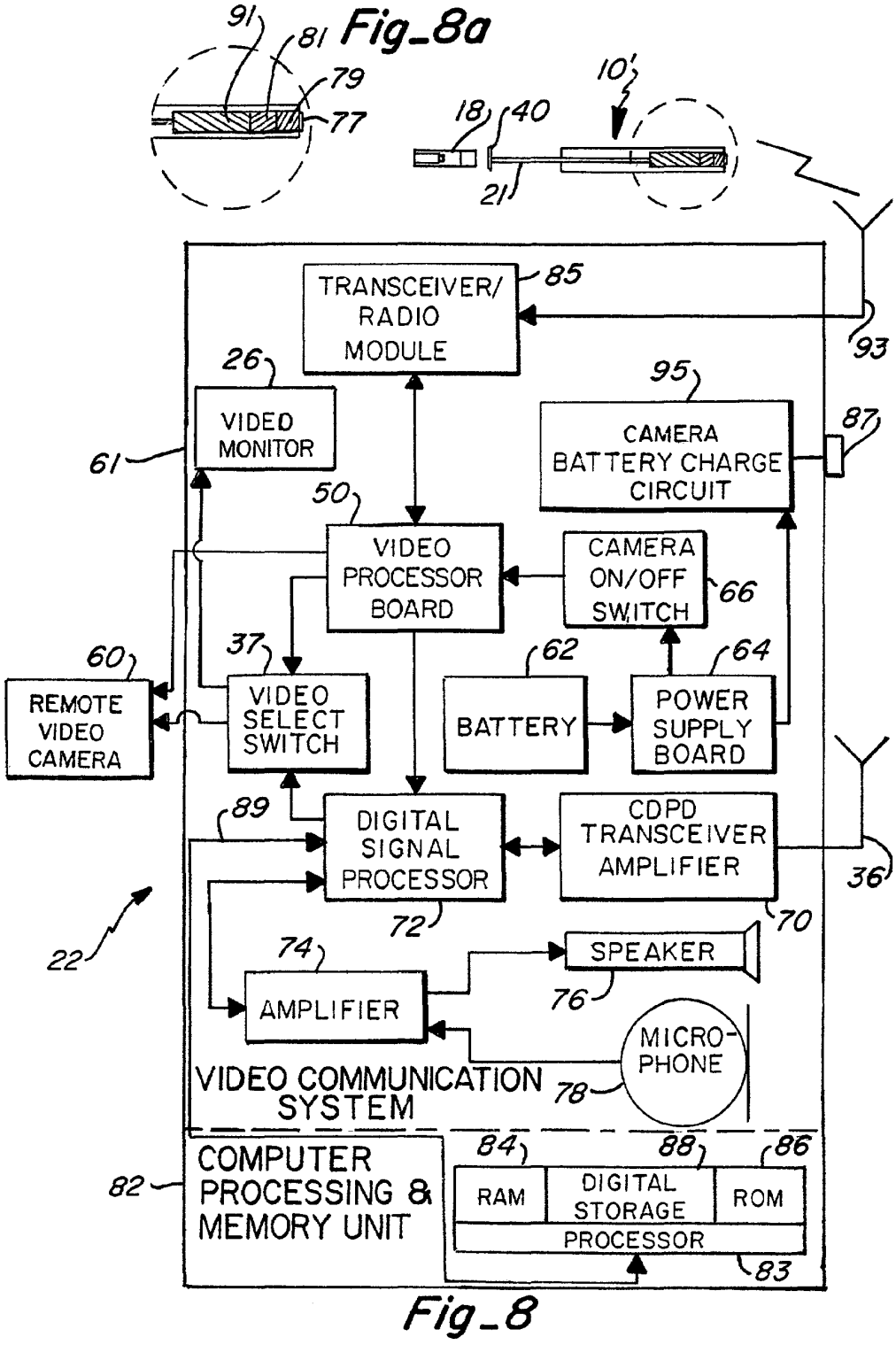
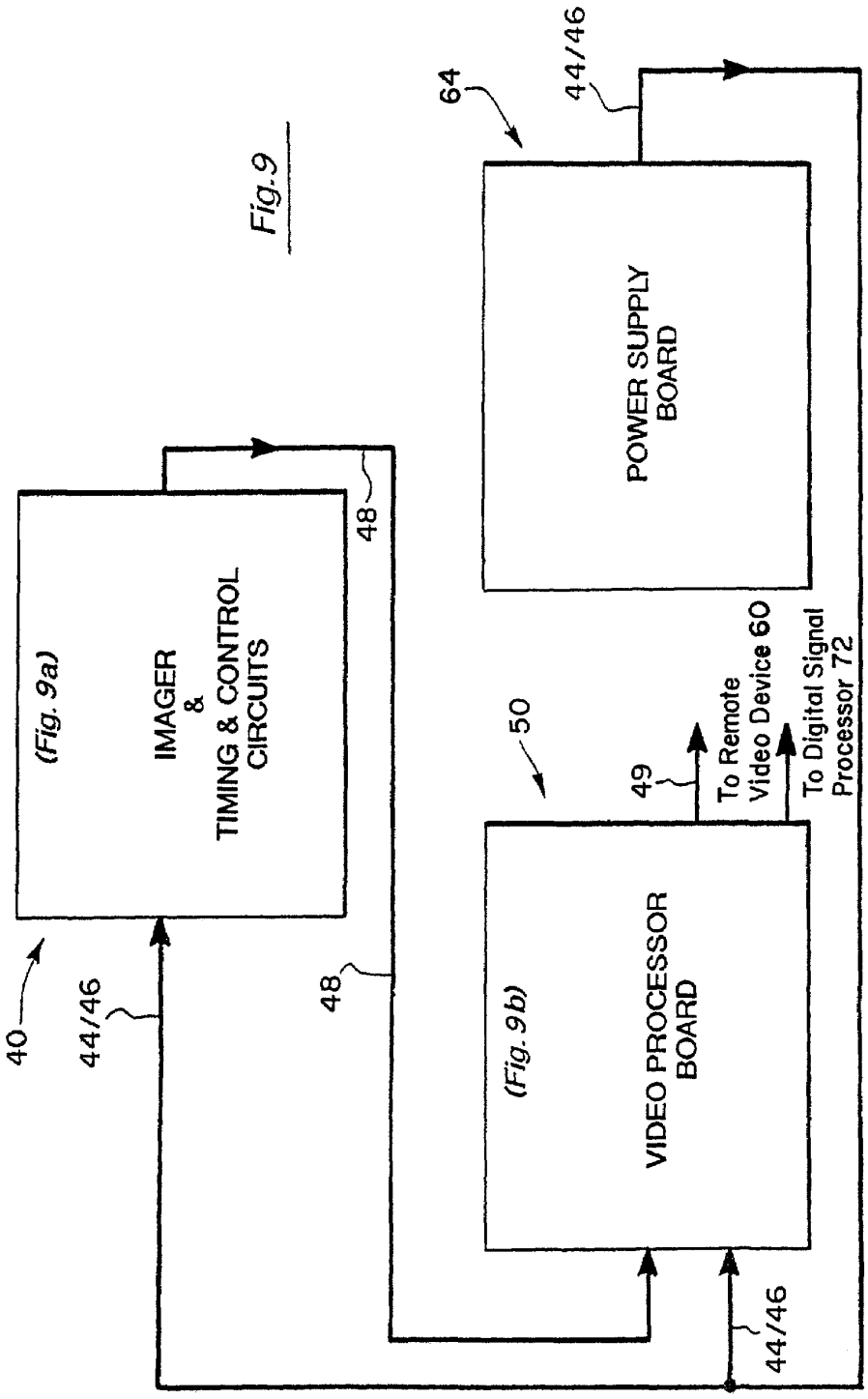

91
81
79
77
18
40
10'
21
TRANSCEIVER/ RADIO MODULE
85
93
26
VIDEO MONITOR
61
95
CAMERA BATTERY CHARGE CIRCUIT
87
50
VIDEO PROCESSOR BOARD
CAMERA ON/OFF SWITCH
66
60
REMOTE VIDEO CAMERA
37
VIDEO SELECT SWITCH
62
BATTERY
64
POWER SUPPLY BOARD
89
DIGITAL SIGNAL PROCESSOR
CDPD TRANSCEIVER AMPLIFIER
36
70
72
22
74
SPEAKER
76
AMPLIFIER
MICRO-PHONE
78
VIDEO COMMUNICATION SYSTEM
82
COMPUTER PROCESSING & MEMORY UNIT
84
88
86
RAM
DIGITAL STORAGE
ROM
PROCESSOR
83

Fig_8a

Fig_8

Fig. 9


64
44/46
POWER SUPPLY BOARD
48
(Fig. 9a)
IMAGER & TIMING & CONTROL CIRCUITS
50
49
To Remote Video Device 60
To Digital Signal Processor 72
40
44/46
48
(Fig. 9b)
VIDEO PROCESSOR BOARD
44/46

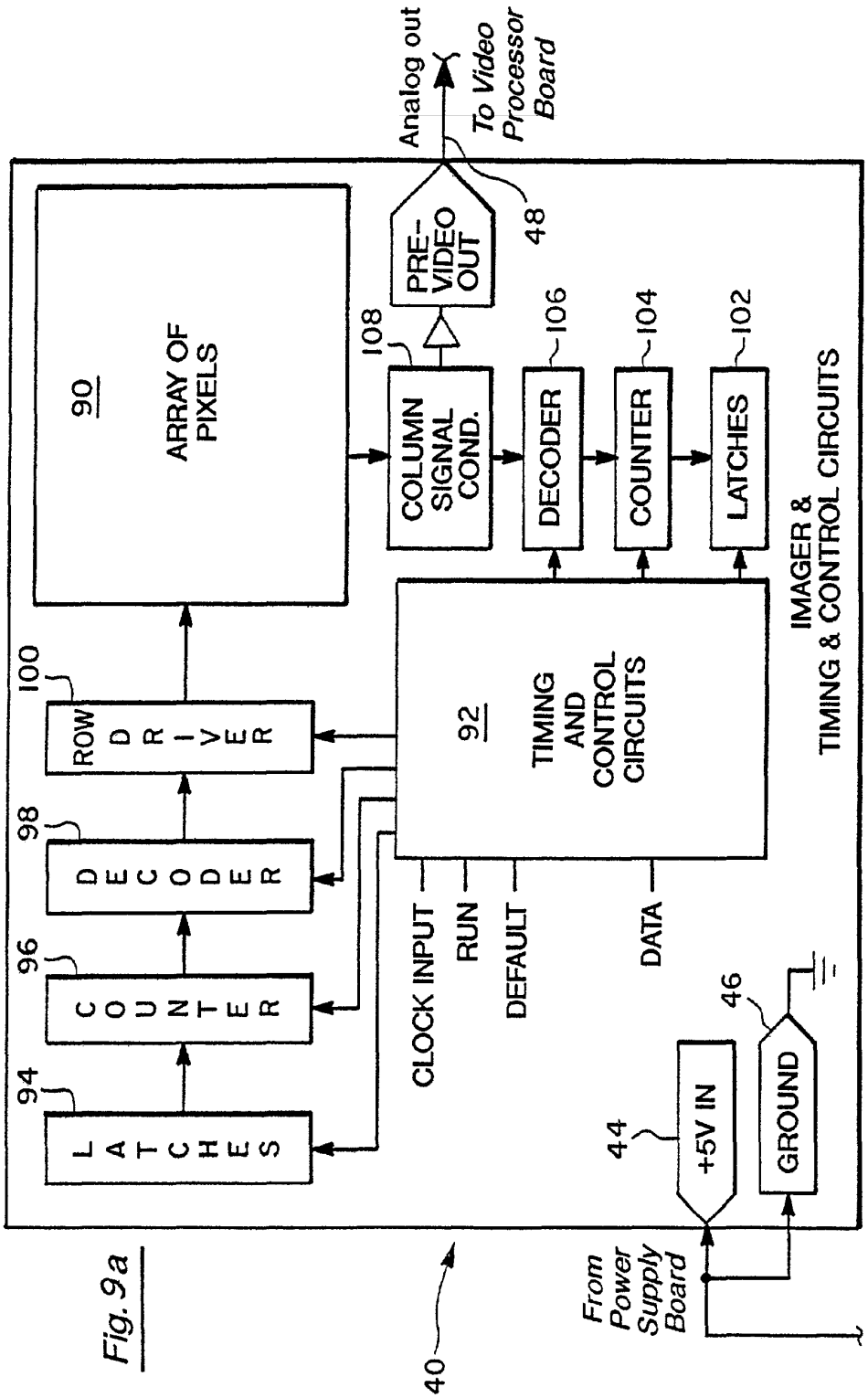

Analog out
To Video Processor Board
48
PRE-VIDEO OUT
108
90
ARRAY OF PIXELS
COLUMN SIGNAL COND.
106
DECODER
104
COUNTER
102
LATCHES
IMAGER & TIMING & CONTROL CIRCUITS
100
ROW DRIVER
92
TIMING AND CONTROL CIRCUITS
98
DECODER
96
COUNTER
94
LATCHES
CLOCK INPUT
RUN
DEFAULT
DATA
46
GROUND
44
+5V IN
From Power Supply Board
40

Fig. 9a

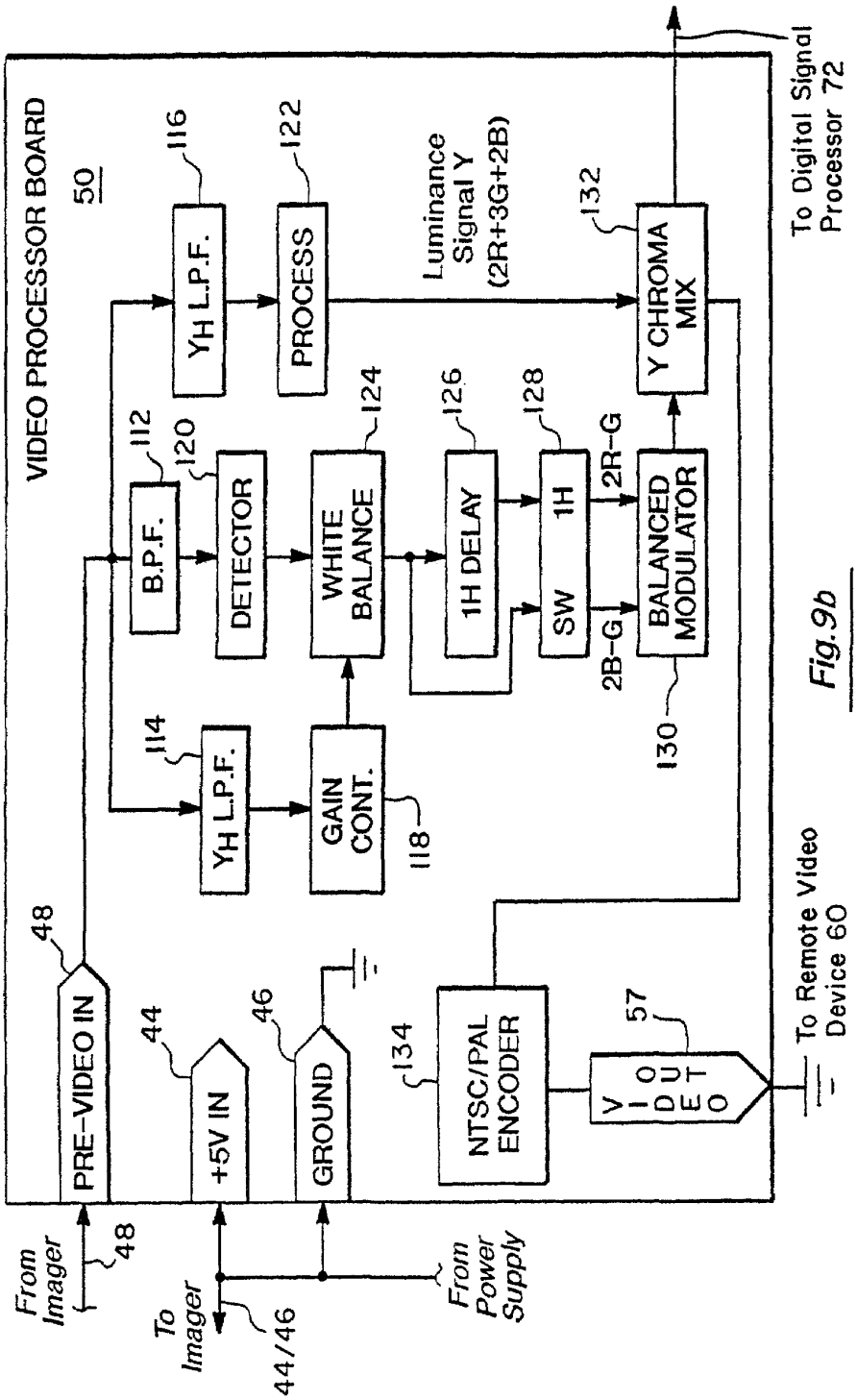

VIDEO PROCESSOR BOARD
50
PRE-VIDEO IN
48
+5V IN
44
GROUND
46
NTSC/PAL ENCODER
134
VIDEO OUT
57
To Remote Video Device 60
To Digital Signal Processor 72
Y CHROMA MIX
132
Luminance Signal Y (2R+3G+2B)
PROCESS
122
YH L.P.F.
116
B.P.F.
112
DETECTOR
120
WHITE BALANCE
124
1H DELAY
126
SW 1H
128
2R-G
2B-G
BALANCED MODULATOR
130
YH L.P.F.
114
GAIN CONT.
118
From Imager
48
To Imager
44/46
From Power Supply

Fig. 9b

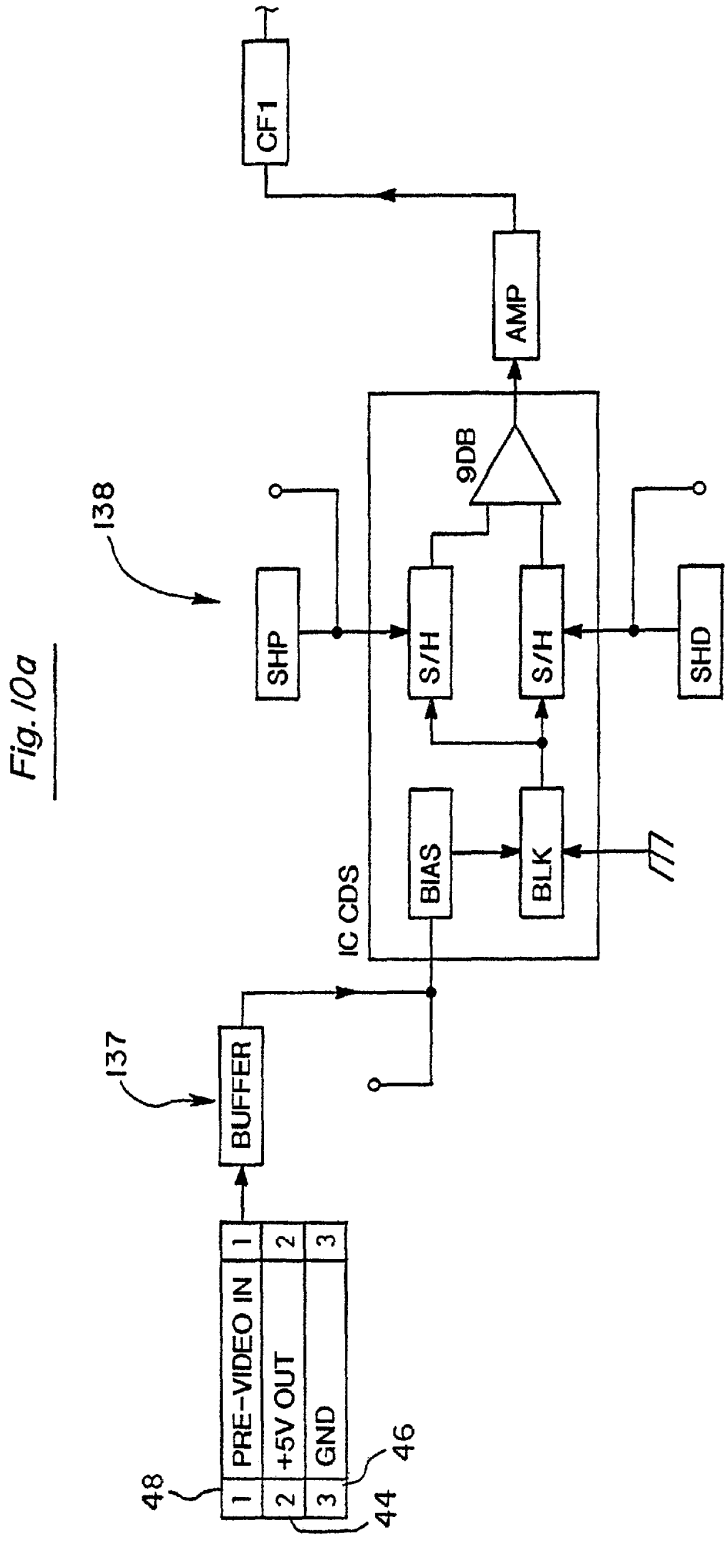

CF1
AMP
9DB
138
SHP
S/H
S/H
SHD
IC CDS
BIAS
BLK
177
137
BUFFER
PRE-VIDEO IN
+5V OUT
GND
1
2
3
48
46
44

Fig. 10a

Fig. 10b

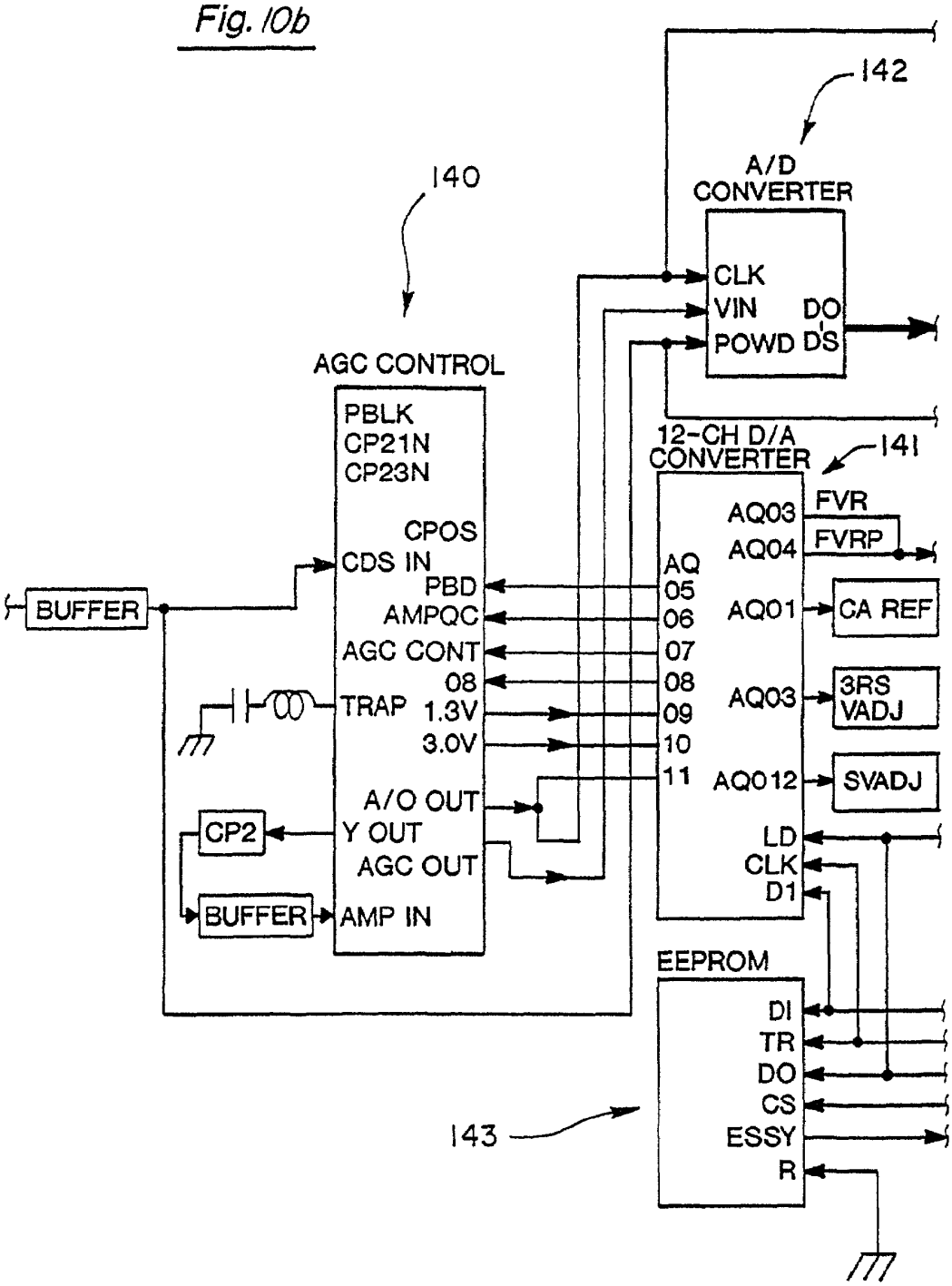
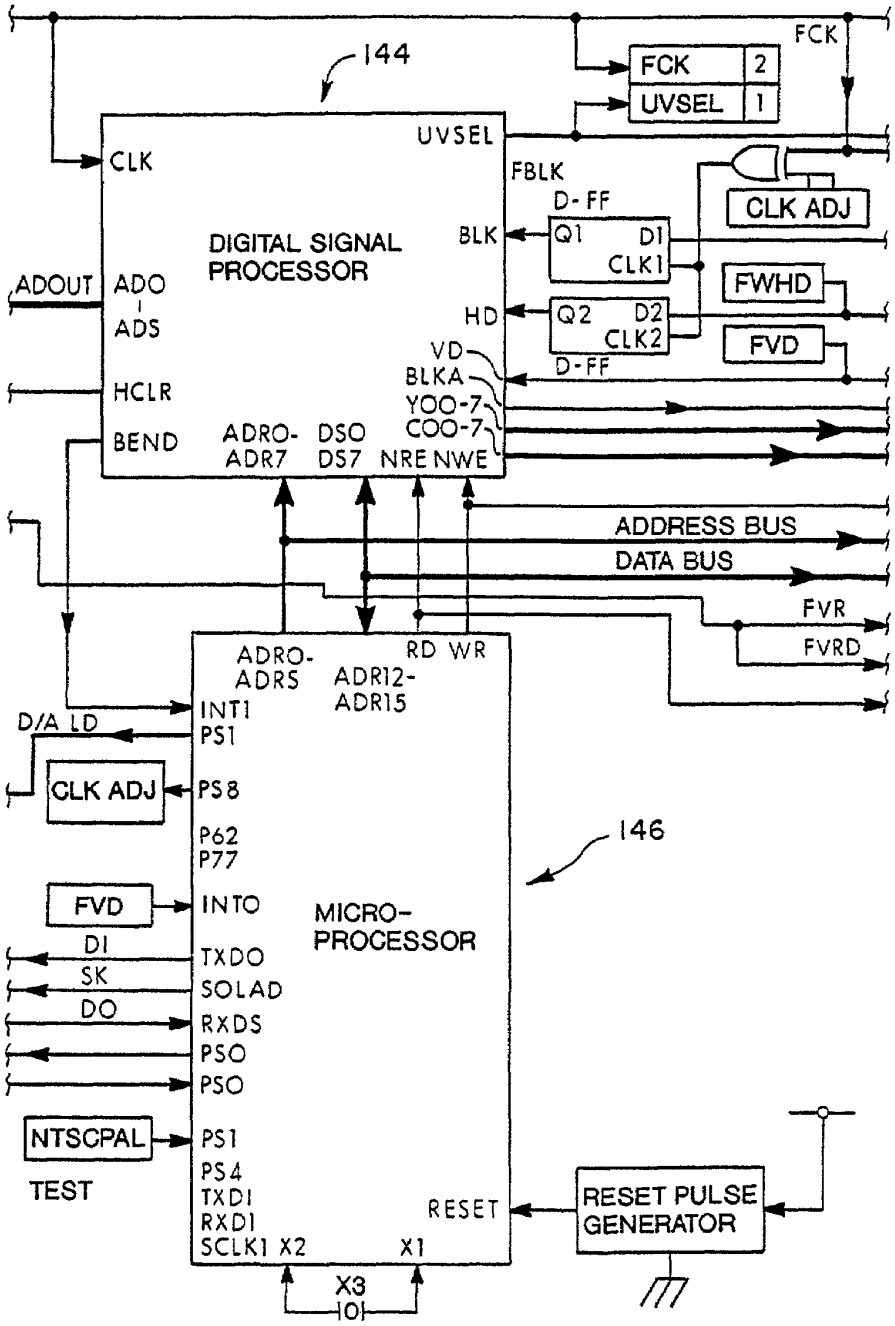

142
A/D CONVERTER
CLK
VIN
POWD
DO
DS
140
AGC CONTROL
PBLK
CP21N
CP23N
CPOS
CDS IN
PBD
AMPQC
AGC CONT
08
TRAP
1.3V
3.0V
A/O OUT
Y OUT
AGC OUT
AMP IN
BUFFER
CP2
BUFFER
12-CH D/A CONVERTER
141
AQ 05
AQ 06
AQ 07
AQ 08
AQ 09
AQ 10
AQ 11
AQ03
AQ04
AQ01
AQ03
AQ012
FVR
FVRP
CA REF
3RS VADJ
SVADJ
LD
CLK
D1
EEPROM
DI
TR
DO
CS
ESSY
R
143

Fig. 10c


144
FCK
FCK 2
UVSEL 1
UVSEL
CLK
FBLK
D-FF
CLK ADJ
DIGITAL SIGNAL PROCESSOR
BLK
Q1 D1
CLK1
FWHD
ADOUT
ADO - ADS
HD
Q2 D2
CLK2
FVD
VD
BLKA
D-FF
HCLR
YOO-7
COO-7
BEND
ADRO- ADR7
DSO DS7
NRE NWE
ADDRESS BUS
DATA BUS
FVR
FVRD
ADRO- ADR5
ADR12- ADR15
RD WR
D/A LD
INT1
PS1
CLK ADJ
PS8
P62
P77
146
FVD
INTO
MICRO- PROCESSOR
DI
TXDO
SK
SOLAD
DO
RXDS
PSO
PSO
NTSCPAL
PS1
TEST
PS4
TXD1
RXD1
RESET
RESET PULSE GENERATOR
SCLK1 X2
X1
X3

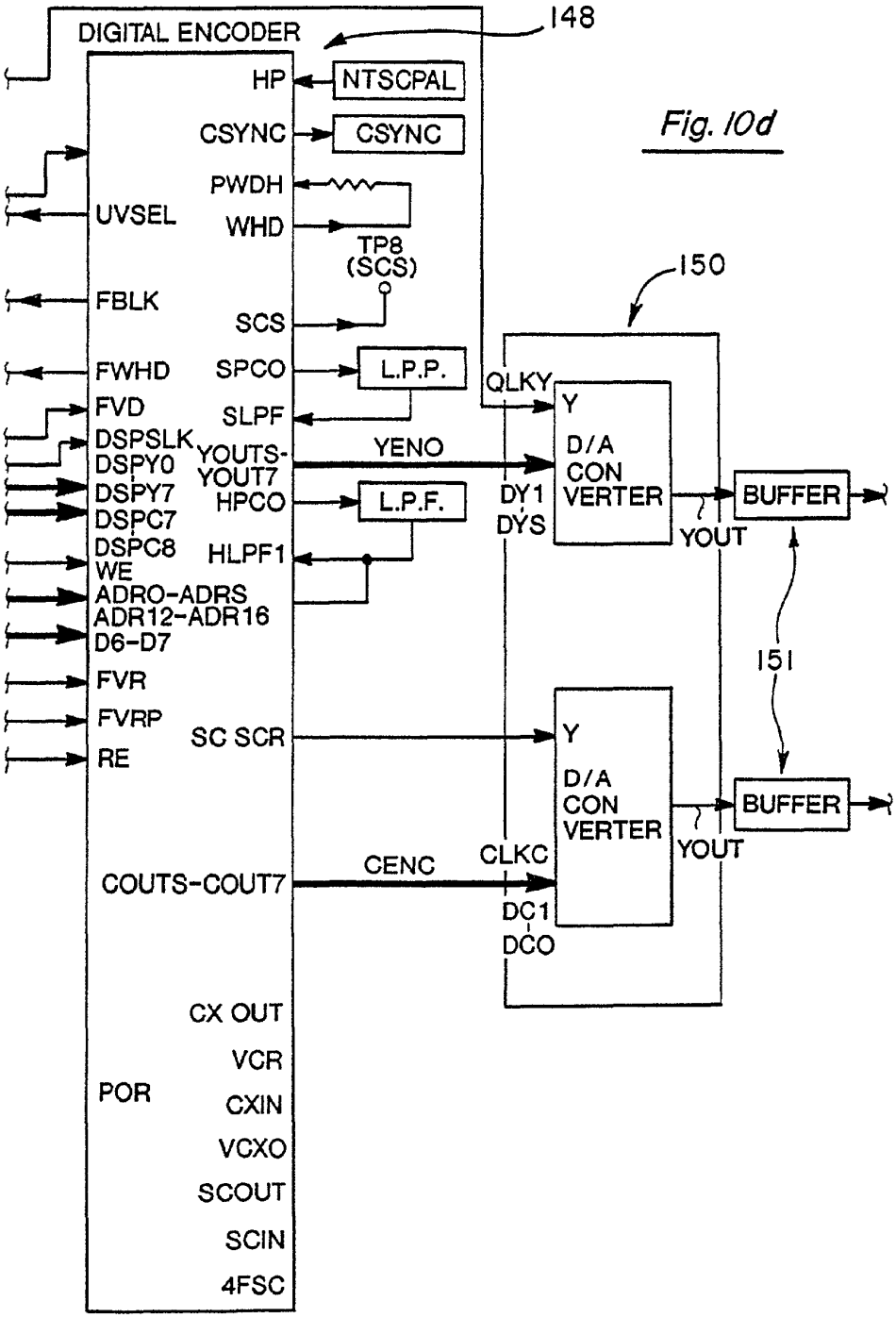

DIGITAL ENCODER
148
HP
NTSCPAL
CSYNC
CSYNC
PWDH
WHD
UVSEL
TP8
(SCS)
FBLK
SCS
FWHD
SPCO
L.P.P.
FVD
SLPF
DSPSLK
DSPY0
DSPY7
DSPC7
DSPC8
WE
ADR0-ADRS
ADR12-ADR16
D6-D7
YOUTS-
YOUT7
YENO
HPCO
L.P.F.
HLPF1
FVR
FVRP
RE
SC SCR
COUTS-COUT7
CENC
CX OUT
VCR
POR
CXIN
VCXO
SCOUT
SCIN
4FSC
150
QLKY
Y
D/A
CON
VERTER
DY1
DYS
BUFFER
YOUT
151
CLKC
DC1
DCO

Fig. 10d

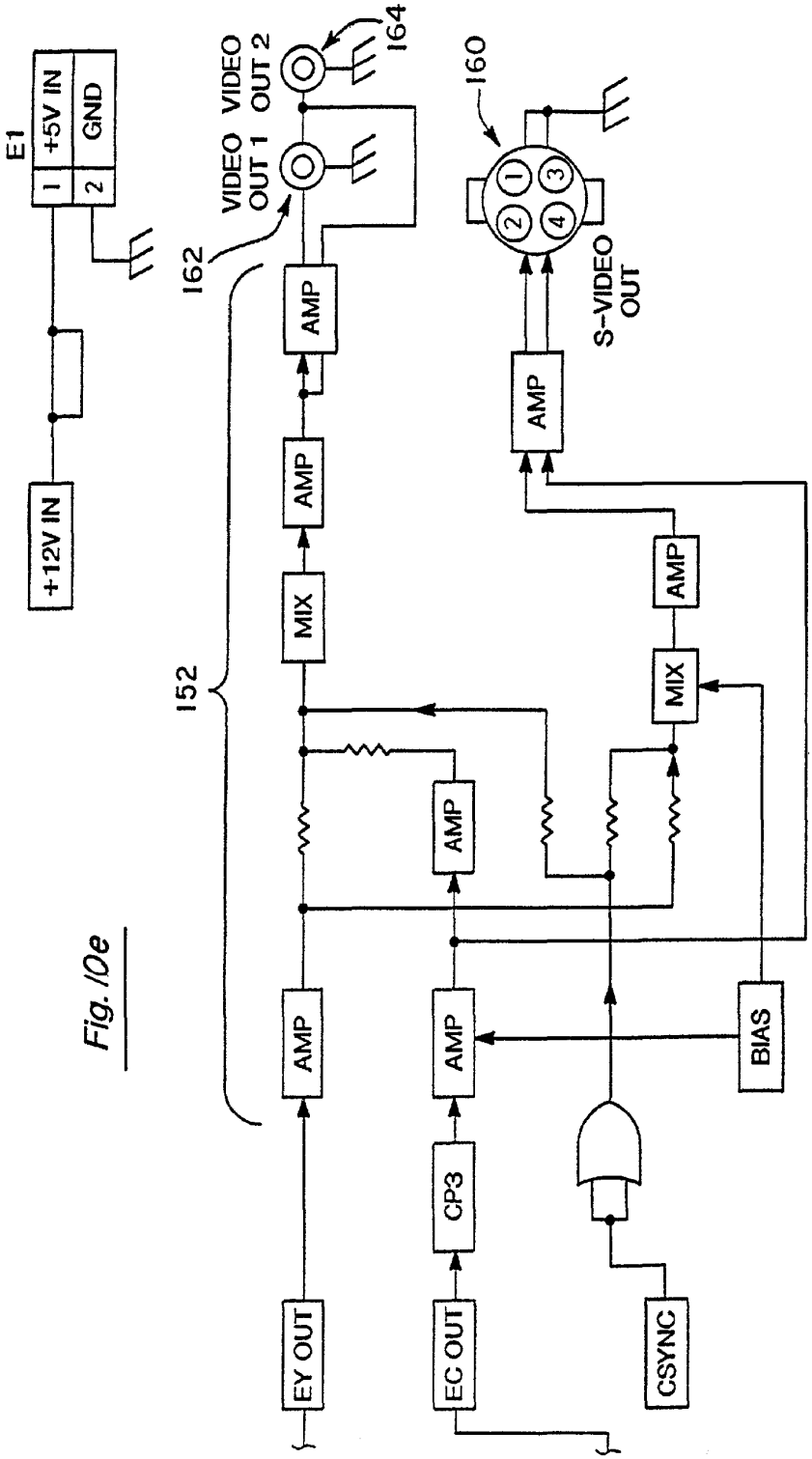

E1
+5V IN
GND
1
2
+12V IN
VIDEO OUT 1
VIDEO OUT 2
164
162
160
S-VIDEO OUT
AMP
MIX
152
BIAS
CP3
EY OUT
EC OUT
CSYNC

Fig. 10e

HAND-HELD COMPUTERS INCORPORATING REDUCED AREA IMAGING DEVICES

This application is a continuation-in-part of U.S. Ser. No. 09/638,976 filed on Aug. 15, 2000 now U.S. Pat. No. 6,424,369, entitled "Hand Held Computers Incorporating Reduced Area Imaging Devices", which is a continuation-in-part of U.S. Ser. No. 09/496,312, filed Feb. 1, 2000 now U.S. Pat. No. 6,275,255, and entitled "Reduced Area Imaging Devices", which is a continuation application of U.S. Ser. No. 09/175,685, filed Oct. 20, 1998 now U.S. Pat. No. 6,043,839 and entitled "Reduced Area Imaging Devices", now U.S. Pat. No. 6,043,839, which is a continuation-in-part of U.S. Ser. No. 08/944,322, filed Oct. 6, 1997 and entitled "Reduced Area Imaging Devices Incorporated Within Surgical Instruments", now U.S. Pat. No. 5,929,901.

TECHNICAL FIELD

This invention relates to solid state image sensors and associated electronics, and more particularly, to solid state image sensors which are configured to be of a minimum size and used within miniature computer systems known as palm top computers, personal digital assistants (PDA), or hand-held computers/organizers.

BACKGROUND ART

The three most common solid state image sensors include charged-coupled devices (CCD) charge injection devices (CID) and photo diode arrays. In the mid-1980s, complementary metal oxide semiconductors (CMOS) were developed for industrial use. CMOS imaging devices offer improved functionality and simplified system interfacing. Furthermore, many CMOS imagers can be manufactured at a fraction of the cost of other solid state imaging technologies.

The CCD device is still the preferred type of imager used in scientific applications. Only recently have CMOS-type devices been improved such that the quality of imaging compares to that of CCD devices. However, there are enormous drawbacks with CCD devices. Two major drawbacks are that CCD devices have immense power requirements, and the amount of processing circuitry required for a CCD imager always requires the use of a remote processing circuitry module which can process the image signal produced by the CCD imager. Also, because of the type of chip architecture used with CCD devices, on-chip processing is impossible. Therefore, even timing and control circuitry must be remoted from the CCD imager plane. Therefore, CCD technology is the antithesis of "camera on a chip" technology discussed below.

One particular advance in CMOS technology has been in the active pixel-type CMOS imagers which consist of randomly accessible pixels with an amplifier at each pixel site. One advantage of active pixel-type imagers is that the amplifier placement results in lower noise levels. Another major advantage is that these CMOS imagers can be mass-produced on standard semiconductor production lines. One particularly notable advance in the area of CMOS imagers including active pixel-type arrays is the CMOS imager described in U.S. Pat. No. 5,471,515 to Fossum, et al. This CMOS imager can incorporate a number of other different electronic controls that are usually found on multiple circuit boards of much larger size. For example, timing circuits, and special functions such as zoom and anti-jitter controls can be placed on the same circuit board containing the CMOS pixel array without significantly increasing the overall size of the host circuit board. Furthermore, this particular CMOS imager requires 100 times less power than a CCD-type imager does. In short, the CMOS imager disclosed in Fossum, et al. has enabled the development of a "camera on a chip."

Passive pixel-type CMOS imagers have also been improved so that they too can be used in an imaging device, which qualifies as a "camera on a chip." In short, the major difference between passive and active CMOS pixel arrays is that a passive pixel-type imager does not perform signal amplification at each pixel site. One example of a manufacturer which has developed a passive pixel array with performance nearly equal to known active pixel devices and compatible with the read out circuitry disclosed in the U.S. Pat. No. 5,471,515 is VLSI Vision, Ltd., 1190 Saratoga Avenue, Suite 180, San Jose, Calif. 95129. A further description of this passive pixel device may be found in the applicant's patent entitled "Reduced Area Imaging Devices Incorporated Within Surgical Instruments," now U.S. Pat. No. 5,986,693, and is hereby incorporated by reference.

In addition to the active pixel-type CMOS imager which is disclosed in U.S. Pat. No. 5,471,515, there have been developments in the industry for other solid state imagers which have resulted in the ability to have a "camera on a chip." For example, Suni Microsystems, Inc. of Mountain View, Calif., has developed a CCD/CMOS hybrid which combines the high quality image processing of CCDs with standard CMOS circuitry construction. In short, Suni Microsystems, Inc. has modified the standard CMOS and CCD manufacturing processes to create a hybrid process providing CCD components with their own substrate which is separate from the P well and N well substrates used by the CMOS components. Accordingly, the CCD and CMOS components of the hybrid may reside on different regions of the same chip or wafer. Additionally, this hybrid is able to run on a low power source (5 volts) which is normally not possible on standard CCD imagers which require 10 to 30 volt power supplies. A brief explanation of this CCD/CMOS hybrid can be found in the article entitled "Startup Suni Bets on Integrated Process" found in *Electronic News*, Jan. 20, 1997 issue. This reference is hereby incorporated by reference for purposes of explaining this particular type of imaging processor.

Another example of a recent development in solid state imaging is the development of a CMOS imaging sensor which is able to achieve analog to digital conversion on each of the pixels within the pixel array. This type of improved CMOS imager includes transistors at every pixel to provide digital instead of analog output that enables the delivery of decoders and sense amplifiers much like standard memory chips. With this new technology, it may, therefore, be possible to manufacture a true digital "camera on a chip." This CMOS imager has been developed by a Stanford University joint project and is headed by Professor Abbas el-Gamal.

A second approach to creating a CMOS-based digital imaging device includes the use of an over-sample converter at each pixel with a one bit comparator placed at the edge of the pixel array instead of performing all of the analog to digital functions on the pixel. This new design technology has been called MOSAD (multiplexed over sample analog to digital) conversion. The result of this new process is low power usage, along with the capability to achieve enhanced dynamic range, possibly up to 20 bits. This process has been developed by Amain Electronics of Simi Valley, Calif. A

brief description of both of the processes developed by Stanford University and Amain Electronics can be found in an article entitled "A/D Conversion Revolution for CMOS Sensor?," September 1998 issue of *Advanced Imaging*. This article is also hereby incorporated by reference for purposes of explaining these particular types of imaging processors.

Yet another example of a recent development with respect to solid state imaging is an imaging device developed by ShellCase, of Jerusalem, Israel. In an article entitled "A CSP Optoelectronic Package for Imaging and Light Detection Applications" (A. Badihi), ShellCase introduces a die-sized, ultrathin optoelectronic package which is completely packaged at the wafer level using semiconductor processing. In short, ShellCase provides a chip scale package (CSP) process for accepting digital image sensors which may be used, for example, in miniature cameras. The die-sized, ultrathin package is produced through a wafer level process which utilizes optically clear materials and completely encases the imager die. This packaging method, ideally suited for optoelectronic devices, results in superior optical performance and form factor not available by traditional image sensors. This article is also incorporated by reference for purposes of explaining ShellCase's chip scale package process.

Yet another example of a recent development with respect to solid state imaging is shown in U.S. Pat. No. 6,020,581 entitled "Solid State CMOS Imager Using Silicon on Insulator or Bulk Silicon." This patent discloses an image sensor incorporating a plurality of detector cells arranged in an array wherein each detector cell as a MOSFET with a floating body and operable as a lateral bipolar transistor to amplify charge collected by the floating body. This invention overcomes problems of insufficient charge being collected in detector cells formed on silicon on insulator (SOI) substrates due to silicon thickness and will also work in bulk silicon embodiments.

The above-mentioned developments in solid state imaging technology have shown that "camera on a chip" devices will continue to be enhanced not only in terms of the quality of imaging which may be achieved, but also in the specific construction of the devices which may be manufactured by new breakthrough processes.

Although the "camera on a chip" concept is one which has great merit for application in many industrial areas, a need still exists for a reduced area imaging device which can be used in even the smallest type of industrial application. Recently, devices known as palm top computers, PDA(s), or hand-held computers have become very popular items. Essentially, these PDAs are miniature computers, small enough to be held in the hand, which have various software programs available to a user including word processing, e-mail, and organization software for addresses/phone books, etc.

One example of a U.S. patent disclosing a type of a PDA includes U.S. Pat. No. 5,900,875. This patent is incorporated herein by reference for purposes of illustrating an example of a PDA including basic functionality for such a device. In a recent article entitled "Palm, Inc. Gets Ready for New Hands" appearing in the *Wallstreet Journal*, a number of soon to be commercially available PDAs are disclosed. One such device disclosed in this article is known as the "Hand Spring Visor Deluxe." This device will soon be available which allows a user to accommodate pagers, MP3 players, still digital cameras and other devices.

It is one general object of this invention to provide a video system in combination with a standard PDA enabling a user to take video images by a very small camera module incorporated within the PDA, view the video images taken on a video view screen incorporated within the PDA, and to have the capability to store video images, download the video images, and send the video images electronically through a communications network.

Another object of this invention is to provide a PDA with the ability to not only transmit video images taken by the camera module, but also to receive video images sent from a remote location via the communications network, and to view such received video images on the video view screen of the PDA. Accordingly, the invention is ideally suited for video teleconferencing.

It is another object of this invention to provide a reduced area imaging device incorporated within a PDA which takes advantage of "camera on a chip" technology, but to rearrange the video processing circuitry in a selective stacked relationship so that the camera module has a minimum profile.

It is yet another object of this invention to provide imaging capability for a PDA wherein the video camera used is of such small size that it can be stored in the PDA when not in use. The camera module is attached to the PDA by a retractable cord which enables the imaging device to be used to image anything at which the camera module is pointed by the user without having to also move the PDA away from the view of the user.

It is yet another object of the invention to provide a video camera with a PDA wherein the camera communicates with a PDA by a wireless link such as a RF radio link so that the camera does not have to be physically connected to the PDA. This wireless connection further enhances the capability to use the camera to shoot video without having to move the PDA or otherwise manipulate the PDA in a manner which detracts from shooting the video.

In all applications, to include use of the imaging device of this invention with a PDA, "camera on a chip" technology can be improved with respect to reducing its profile area, and incorporating such a reduced area imaging device within a PDA such that minimal size and weight is added to the PDA, and further that the imaging device can be used to image selected targets by the user.

DISCLOSURE OF THE INVENTION

In accordance with the present invention, reduced area imaging devices are provided in combination with a hand-held computer or PDA. The term "imaging device" as used herein describes the imaging elements and processing circuitry which is used to produce a video signal which may be accepted by both a standard video device such as a television or video monitor accompanying a personal computer, and a small LCD screen which is incorporated within the PDA. The term "image sensor" as used herein describes the components of a solid state imaging device which captures images and stores them within the structure of each of the pixels in the array of pixels found in the imaging device. As further discussed below, the timing and control circuits can be placed either on the same planar structure as the pixel array, in which case the image sensor can also be defined as an integrated circuit, or the timing and control circuitry can be placed remote from the pixel array. The terms "video signal" or "image signal" as used herein, and unless otherwise more specifically defined, refer to an image which at some point during its processing by the imaging device, is found in the form of electrons which have been placed in a specific format or domain. The term "processing circuitry" as used herein refers to the electronic components within the imaging device which receive the image signal from the

image sensor and ultimately place the image signal in a usable format. The terms "timing and control circuits" or "timing and control circuitry" as used herein refer to the electronic components which control the release of the image signal from the pixel array.

In a first embodiment of the PDA, the imaging device connects to the PDA by a cable or cord that may retract within the housing of the PDA. Thus in this embodiment, the camera is tethered to the PDA. In a second embodiment, the imaging device does not have to be physically connected to the PDA; rather, a wireless RF link or other acceptable wireless technology is used so that video signals produced by the imaging device may be transmitted to and received by the PDA. One particularly advantageous wireless technology usable with the PDA of this invention is known as "Bluetooth". Another recent wireless technology which is usable with the invention is a wireless protocol known as "IEEE 802.15.3". This wireless standard is developing under the joint efforts of Kodak, Motorola, Cisco and the International Electronic and Electrical Engineers Standards Association (IEEE) Wireless Personal Area Network Working Group (WPAN). Bluetooth technology provides a universal radio interface in the 2.4 GHz frequency band that enables portable electronic devices to connect and communicate wirelessly via short-range ad hoc networks. Bluetooth radios operate in an unlicensed Instrumentation, Scientific, Medical (ISM) band at 2.4 GHz. Bluetooth is a combination of circuit and packet switching. Slots can be reserved for synchronous packets. Each packet is transmitted in a different hop frequency. A packet nominally covers a single slot, but can be extended to cover up to five slots. Bluetooth can support an asynchronous data channel, up to three simultaneous synchronous voice channels, or a channel that simultaneously supports asynchronous data and synchronous voice. Spectrum spreading is used to facilitate optional operation at power levels up to 100 mW worldwide. Spectrum spreading is accomplished by frequency hopping in 79 hops displaced by 1 MHz, starting at 2.402 GHz and stopping at 2.480 GHz. The maximum frequency-hopping rate is 1600 hops per second. The nominal link range is 10 centimeters to 10 meters, but can be extended to more than 100 meters by increasing the transmit power. A shaped, binary FM modulation is applied to minimize transceiver complexity. The gross data rate is 1 Mb/second. A time division duplex scheme is used for full-duplex transmission. Additional technical information describing the Bluetooth global specification is found on the world wide web at www.bluetooth.com. Additional information regarding the technical specification for the IEEE 802.15.3 standard may be found at http://www.ieee802.org/15, under the link for Task Force Three (TG3).

In a first arrangement of the imaging device, the image sensor, with or without the timing and control circuitry, may be placed at the distal tip of a very small video camera module which communicates with the PDA by a wireless RF link or is attached by a cable or cord to the PDA, or the camera module communicates with the PDA by a wireless RF link while the remaining processing circuitry may be placed within the housing of the PDA.

In a second arrangement of the imaging device, the image sensor and the processing circuitry may all be placed in a stacked arrangement of miniature circuit boards and positioned at the distal tip of the video camera module. In this second arrangement, the pixel array of the image sensor may be placed by itself on its own circuit board while the timing and control circuitry and processing circuitry are placed on one or more other circuit boards, or the circuitry for timing and control may be placed with the pixel array on one circuit board, while the remaining processing circuitry can be placed on one or more of the other circuit boards.

In yet another alternative arrangement of the imaging device, the pixel array, timing and control circuits, and some of the processing circuitry can be placed near the distal end of the video camera module with the remaining part of the processing circuitry being placed in the housing of the PDA.

For the arrangement or configuration of the imaging device that calls for the array of pixels and the timing and control circuitry to be placed on the same circuit board, only one conductor is required in order to transmit the image signal to the video processing circuitry. When the timing and control circuits are incorporated onto other circuit boards, a plurality of connections are required in order to connect the timing and control circuitry to the pixel array, and then the one conductor is also required to transmit the image signal back to the video processing circuitry.

As mentioned above, the invention disclosed herein can be considered an improvement to a PDA wherein the improvement comprises a video system. The video system would include the video view screen or monitor attached to the PDA, the camera module, as well as supporting video processing circuitry for the imaging device. In yet another aspect, the invention disclosed herein can also be considered an improvement to a PDA wherein the improvement comprises a novel imaging device, preferably of CMOS construction. For this improvement comprising the imaging device, the imaging device includes the array of pixels, and the supporting video processing circuitry for providing a video ready signal.

In yet another aspect, the invention disclosed herein can also be considered an improvement to a PDA wherein the improvement comprises an imaging device which utilizes a wireless standard in order to transmit video images to the PDA.

This video ready signal may be formatted by the video processing circuitry for viewing on a NTSC/PAL compatible device such as television, or for viewing on a VGA compatible device such as a monitor of a personal computer. Of course, the video ready signal is formatted for viewing the video images on the video view screen incorporated within the PDA.

In yet another aspect, the invention disclosed herein can also be considered an improvement to a PDA wherein the improvement comprises a combination of a video system, and wireless telephone communication means for transmitting and receiving both audio and video signals. In this aspect, the invention has functionality for transmitting and receiving audio and video signals via the communications network. One example of a U.S. patent disclosing wireless remote communications between a personal computer and a PDA or miniature hand held computer is U.S. Pat. No. 6,034,621. This patent is hereby incorporated by reference in its entirety for purposes of disclosing means by which data can be exchanged between the hand held computer and a personal computer, to include video and audio signals. The specific example in this patent which readily lends itself to the communication network incorporated within this invention is found at FIG. 4 of this '621 patent. The discussion further below outlines this particular communication network.

In yet another aspect, the invention disclosed herein can also be considered an improvement to a PDA wherein the improvement comprises a video system, and a standard wireless telephone communication means for transmitting and receiving audio signals. In this aspect, the PDA simply

includes a standard wireless/cellular phone connected externally on the PDA which enables the user to conduct well-known wireless/telephone communications. This wireless/cellular communication means can be in addition to the wireless telephone communication means for transmitting and receiving both audio and video signals discussed immediately above with respect to the U.S. Pat. No. 6,034,621.

Another example of a U.S. patent disclosing basic mobile phone technology including a discussion of basic phone circuitry is U.S. Pat. No. 6,018,670. This patent is hereby incorporated by reference in its entirety for purposes of disclosing standard or basic mobile phone technology and supporting circuitry.

Accordingly, the invention disclosed herein has utility with respect to an overall combination of elements, as well as various sub-combinations of elements.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an enlarged fragmentary partially exploded perspective view of the distal end of the camera module which is used in conjunction with the PDA, specifically illustrating the arrangement of the image sensor with respect to the other elements of the camera module;

FIG. **1***a* is an enlarged exploded perspective view illustrating another configuration of the image sensor wherein video processing circuitry is placed behind and in longitudinal alignment with the image sensor;

FIG. **2** is a perspective view of the PDA in a first embodiment incorporating the reduced area imaging device of this invention;

FIG. **3** illustrates the PDA of FIG. **2** wherein the camera module is in the retracted position;

FIG. **4** is an overall schematic diagram of the functional electronic components in the first embodiment which make up both the PDA and the reduced area imaging device wherein communications are achieved by wireless/cellular technology for video teleconferencing via the world wide web which is well-known as a global communications network;

FIG. **5** is a schematic diagram illustrating an example communications network which can be used for data transfer of text, audio, and visual signals between the PDA and a personal computer which is in communication with the world wide web;

FIG. **6***a* is a perspective view of the PDA in the first embodiment illustrated in combination with an externally attached wireless/cellular phone;

FIG. **6***b* is another perspective view of the combination of FIG. **6***a* illustrating the combination opened to expose the PDA;

FIG. **7** is a perspective view of the PDA in a second embodiment wherein the camera module utilizes a wireless technology, thus the camera module may be physically separated from the PDA during operation, but can still be housed within the PDA for storage and for recharge of the battery of the camera module;

FIG. **8** is an overall schematic diagram, similar to FIG. **4**, of the functional components which make up the PDA and a simplified cross sectional view of the camera module in the second preferred embodiment wherein the camera module communicates with the PDA via a wireless link;

FIG. **8***a* is an enlarged view of some of the components of the camera module, specifically, the components used in the wireless link with the PDA;

FIG. **9** is a more detailed schematic diagram of the functional electronic components, which make up the imaging device;

FIG. **9***a* is an enlarged schematic diagram of a circuit board/planar structure, which may include the array of pixels and the timing and control circuitry;

FIG. **9***b* is an enlarged schematic diagram of a video processing board/planar structure having placed thereon the processing circuitry which processes the pre-video signal generated by the array of pixels and which converts the pre-video signal to a post-video signal which may be accepted by an NTSC/PAL compatible video device; and

FIGS. **10***a*–**10***e* are schematic diagrams that illustrate an example of specific circuitry which may be used to make the video processing circuitry of the imaging device.

BEST MODE FOR CARRYING OUT THE INVENTION

In accordance with the invention, as shown in FIG. **1**, a camera module **10** is provided which incorporates a reduced area imaging device **11**. As further discussed below, the elements of the imaging device **11** may all be found near one location, or the elements may be separated from one another and interconnected by the appropriate wired connections. The array of pixels making up the image sensor captures images and stores them in the form of electrical energy by conversion of light photons to electrons. This conversion takes place by the photo diodes in each pixel which communicate with one or more capacitors which store the electrons. Specifically, the camera module **10** includes an outer tube/sheath **14** which houses the components of the imaging device. The camera module is shown as being cylindrical in shape having a window **16** sealed at the distal end of the camera module. A retractable cable **12** extends from the proximal end of the camera module **10**. A shielded cable **21** is used to house the conductors which communicate with the imaging device **11**. The shielded cable **21** is then housed within the retractable cable **12**. A lens group **18** is positioned at the distal end of the camera module to enable an image to be appropriately conditioned prior to the image impinging upon the imaging device **11**. Also shown is a focusing ring **20** which enables the lens group **18** to be displaced distally or proximally to best focus an image on the imaging device **11**.

Now referring to FIGS. **2** and **3**, a PDA **22** in a first embodiment is shown which incorporates the camera module **10**. In basic terms, the PDA **22** is a miniature hand-held computer incorporating a video system enabling video to be taken by the camera module, and viewed on the video view screen **26**, as well as enabling images to be stored and downloaded on a miniature computer disc (not shown) used with the PDA. Also discussed further below is the ability to transmit and receive audio and video signals.

Beginning first with a description of the basic components of the PDA **22**, it includes a housing **24** which hold the components of the PDA and the video system. Cable **12** is housed within the housing **24** when in the retracted position. A spring biased spool (not shown) or some other known retracting device is mounted within the housing **24** enabling the cable **12** to be extended or retracted. A plurality of controls is provided enabling the user to manipulate the functions of the PDA. These are shown as buttons **34** on the housing **24**. The video view screen **26** is used for displaying video images taken by the camera module **10**, or for viewing incoming video signals received from a remote location. A command screen **28** is provided which allows a user to select

programs with a stylus (not shown). A video capture button **30** is provided which allows a user to capture a still video image taken by the camera module **10**. A video store button **32** is also provided which enables a captured video image to be stored within the digital memory of the PDA, as further discussed below. An opening or cavity **35** is provided which allows the camera module **10** to be stored, along with cable **12** within the housing **24**. As shown in FIG. **3**, the camera module **10** is in the stored or retracted position. The antenna **36** allows for enhanced transmission and reception of incoming or transmitted/outgoing audio and video signals. A video select switch **37** is provided enabling a user to view either video images taken by the camera module **10**, or for viewing incoming video images. The video view screen **26** may be a liquid crystal display (LCD) type, or any other well-known display device of high resolution which has low power requirements, and has minimum size requirements as well.

An example of a manufacture of such a miniature LCD monitor includes DISPLAYTECH of Longmont, Colo. DISPLAYTECH manufactures a miniature reflective display that consists of ferroelectric liquid crystal (FLC) applied to a CMOS integrated circuit. The reflective display is a VGA display panel having low voltage digital operation, low power requirements, and full color operation. One of their specific products includes the LightCaster™ VGA Display Panel, Model LDP-0307-MV1. This is but one example of a LCD monitor that is available and usable within the invention herein described.

A camera on/off switch **66** is provided enabling the user to turn the video system on or off. Also shown in FIGS. **2** and **3** is a speaker **76** and a microphone **78** which are used for sending and receiving audio signals in the conventional manner as with a wireless/cellular telephone. A further description of speaker **76** and microphone **78** is found below.

Referring back to FIGS. **1** and **1***a*, the imaging device **11** includes an image sensor **40**. FIG. **1** illustrates that the image sensor **40** can be a planar and square shaped member, or alternatively, planar and circular shaped to better fit within outer tube **14**. In the configuration of the imaging device in FIGS. **1** and **1***a*, there are only three conductors which are necessary for providing power to the image sensor **40**, and for transmitting an image from the image sensor **40** back to the processing circuitry found within the phone housing **24**. Specifically, there is a power conductor **44**, a grounding conductor **46**, and an image signal conductor **48**, each of which are hardwired to the image sensor **40**. Thus, shielded cable **21** may simply be a three conductor, 50 ohm type cable.

Image sensor **40** can be as small as 1 mm in its largest dimension. However, a more preferable size for most PDA applications would be between 4 mm to 8 mm in the image sensor's largest dimension (height or width). The image signal transmitted from the image sensor **40** through conductor **48** is also herein referred to as a pre-video signal. Once the pre-video signal has been transmitted from image sensor **40** by means of conductor **48**, it is received by video processing board **50**, as shown in FIG. **6***b*. Video processing board **50** then carries out all the necessary conditioning of the pre-video signal and places it in a form, also referred to herein as a video ready signal, so that it may be viewed directly on a remote video device such as a television or standard computer video monitor. In order for the pre-video signal to be viewed on the video view screen/monitor **26**, the pre-video signal is further conditioned by a digital signal processor **72**, as further discussed below. The video signal produced by the video processing board **50** can be viewed by an NTSC/PAL compatible video device (such as a television) which connects to the PDA through a remote jack. This video signal produced by board **50** can be further defined as a post-video signal.

FIG. **1** illustrates an arrangement wherein the image sensor **40** is placed by itself adjacent the distal end of the camera module **10**. Alternatively, some or all of the video processing circuitry may be placed in adjacent circuit boards directly behind the image sensor **40**. Accordingly, la illustrates video processor board **50** aligned directly behind the image sensor **40**. A plurality of pin connectors **52** can be used to interconnect image sensor **40** to video processor board **50**. Depending upon the specific configuration of image sensor **40**, pin connectors **52** may be provided for structural support only, and/or to provide a means by which image signals are transmitted between image sensor **40** and board **50**. Additionally, digital signal processor **72** could also be placed behind image sensor **40** and behind video processing board **50**. Accordingly, the image sensor, and all supporting video processing circuitry could be placed at the distal end of the camera module **10**. However, because of the ample space within housing **24**, it may be preferable to place at least some of the video processing circuitry within housing **24**. In the case of FIG. **1***a*, the conductor **49** represents the conductor which may carry the post-video signal for direct connection with a remote video device **60** such as a television or computer monitor. As also discussed further below with respect to the first embodiment, placement of the digital signal processor **72** at the distal tip of the camera module behind the video processing board **50** would also enable yet another conductor (not shown) to connect directly to the video monitor **26** for transmitting a video signal to the video monitor **26**.

Again referring to FIGS. **1** and **1***a*, the area which is occupied by image sensor **40** may be defined as the profile area of the imaging device and which determines its critical dimensions. If it is desired to place video processing circuitry adjacent the image sensor **40** at the distal end of the camera module **10**, such circuitry must be able to be placed on one or more circuit boards that are longitudinally aligned with image sensor **40** along longitudinal axis XX. If it is not important to limit the size of the profile area, then any circuitry placed behind image sensor **40** can be aligned in an offset manner, or may simply be larger than the profile area of image sensor **40**. In the configuration shown in FIG. **1***a*, it is desirable that elements **40** and **50** be approximately the same size so that they may uniformly fit within the distal end of outer tube **14**.

Now referring to the first embodiment of FIG. **4**, a further explanation is provided of the basic electronic components of the PDA **22**. The PDA **22** of this invention includes functionality normally found in multiple devices. Specifically, the PDA **22** includes the computing capability of a PDA, a mobile/wireless phone, communication means for connection to a computer network such as the worldwide web, and a video system. The PDA **22** may be separated into two major groups, namely, a video and communication system **61**, and a computer processing and memory unit **82**. Both of these are discussed in further detail below.

As shown in FIG. **4**, a conventional lithium ion battery **62** is provided which communicates with power supply board **64**. Power supply board **64** conditions various power outputs to the components of the device, to include power to the video components. In the preferred imaging device of this invention, the power to the imaging device may simply be direct current of between about 1.5 to 12 volts, depending upon the power requirements of the imaging device. A

camera on/off switch **66** must be set to the "on" position in order to activate the camera module **10**. The video processor board **50** then transfers power to supplies the camera module **10**, and also receives the analog pre-video signal back from the camera module, as further discussed below. After processing of the pre-video signal at the video processor board **50**, the video signal is video ready, meaning that it may then be directly viewed on a remote compatible video device **60**, such as a television or computer monitor. A video port **54** can be provided on the housing **24** enabling a user to take a standard video jack (not shown) and interconnect the PDA with the video port of the remote video device. The video format for such remote video devices includes NTSC/PAL and VGA; thus, the video signal processed by video processor board **50** creates the video ready signals for use with these remote video devices. For purposes of viewing images on the monitor **26**, the pre-video signal is farther processed into a digital format within video processor board **50**, preferably an 8 bit component video signal format that is commonly referred to as "YUV 4:2:2." This video format easily lends itself to video compression. This 8-bit digital video signal is then sent to the digital signal processor **72** which performs two functions relevant to the video signal. The digital signal processor **72** further converts the signal into a format that is compatible with the driver circuitry of the video monitor **26**. Secondly, the digital signal processor **72** compresses the YUV signal using a common video compression format, preferably JPEG. The JPEG encoded video signal is then mixed with the audio signal created by microphone **78** and amplifier **74**, and the resulting high frequency carrier signal may then be passed onto the transceiver/amplifier section **70** for transmission. It is to be understood that the transceiver/amplifier **70** is intended for communication with well-known wide area wireless communication networks. It is also contemplated within the spirit and scope of this invention that the PDA **22** be capable of communication with computer networks to include the worldwide web. Accordingly, the invention is well adapted for conducting video teleconferencing that is normally conducted with desktop computers and supplemental video equipment. The transceiver/amplifier section also modulates the carrier signal prior to transmission. Depending upon the position of video switch **37**, the video signal from digital signal processor **72** is either sent to the monitor **26**, or is sent to the transceiver/amplifier section **70** for transmission. As also shown, the antenna **36** is used for enhancement of reception and transmission of transmitted and received carrier signals.

The transceiver/amplifier section **70** also serves as a receiver that receives an incoming carrier signal. This incoming signal is then demodulated within section **70**, the video and audio components of the incoming signal are separated, and then these separated signals are then sent to the digital signal processor **72** which performs video decompression. Then, the decompressed video signal is sent to the monitor **26** for viewing (if the video switch **37** is placed in that selected mode). The decompressed audio signal is sent to the amplifier **74**, and then to the speaker **76**.

FIG. **4** shows the transceiver/amplifier section **70** as being a cellular digital packet data system (CDPD) type transceiver. This particular transceiver/amplifier **70** could be the same as that disclosed in the U.S. Pat. No. 6,034,621. A cellular digital packet system is a wireless standard providing two-way, 19.2 KBPS packet data transmission over existing cellular telephone channels.

The video switch **37** may simply be a momentary, spring loaded, push button-type switch. When the video switch **37** is not depressed, incoming video, which is received via the antenna **36**, is processed as discussed above in the transceiver/amplifier section **70** and digital signal processor **72**, and then sent to the monitor **26**. When the video switch **37** is depressed and held, the video signal produced from the camera module **10** is processed as discussed above, and ultimately sent to the monitor **26** for viewing by the user. An operator can cycle the switch **37** between the two positions in order to selectively choose whether to view incoming or outgoing video.

FIG. **5** illustrates a communications network that can be used by the invention. A communications network of this type is disclosed in the U.S. Pat. No. 6,034,621, and is discussed specifically therein at FIGS. 3 and 4 of that patent. FIG. **5** illustrates a CDPD base station **182** with a remote computer **188** utilizing a direct connection to the CDPD base station **182** via a modem **186** with a dial-up connection to the public switch telephone network (PSTN) **184**. The CDPD base station **182** includes an antenna **181**. The remote computer **188** can be a personal computer, a server, or any other well-known stand-alone computer.

Referring back to FIG. **4**, the computer processing and memory unit **82** which allows the PDA **22** to achieve basic word processing, etc., includes a microprocessor **83**, RAM **84**, ROM **86**, and digital storage **88**. Digital storage **88** is provided for storing the formatted images taken by the camera module **10**. The RAM **84**, microprocessor **83**, and ROM **86** are conventional or standard components as found in existing PDAs. An input/output bus **89** is provided which allows video signals to be stored or otherwise manipulated within the computer processing and memory unit **82**. Accordingly, video taken by camera module **10** can be downloaded to digital storage **88**. Also, existing image data stored in digital storage **88** could be viewed on video monitor **26**.

FIGS. **6***a* and **6***b* illustrate another combination of the invention wherein the PDA **22** is simply combined with an externally mounted cellular telephone **190**. The cellular phone **190** is a commercially available cellular/wireless telephone. As shown, the telephone includes the standard keypad **194**, visual display **196**, and antennae **198**. The phone **190** is secured to the PDA **22** as by mounting means **192**, which is shown in the preferred embodiment as a piano-type hinge. Thus, the PDA is altered very simply by providing means by which a cellular telephone can be attached to the PDA. This enables the user to hold both the PDA and cellular telephone in one hand while manipulating the PDA or phone **190** as desired with the other hand. All of the telephone circuitry for phone **190** is housed within the phone itself, and there is no circuitry within the PDA which is used within the phone **190**.

The actual size of the phone **190** is smaller than the PDA **22**. However, in order to create a uniform edged combination, the phone **190** is housed in a larger housing **200** which essentially matches the dimensions of housing **24**. Additionally, a peripheral flange could be provided on the inner surface of housing **200** which comes into contact with housing **24** in the closed position of FIG. **6***a* which would prevent inadvertent activation of the control buttons on the PDA **22**.

Now referring to FIGS. **7** and **8**, the second embodiment of the PDA is illustrated that utilizes a wireless camera module **10'**. As with the first embodiment, the camera module **10'** is cylindrical shaped and can be stored within hole or orifice **35**. Thus, exteriorly, the PDA **22** appears the same, along with camera module **10'** with the exception that there is no cable or cord interconnecting the camera module

10' to the PDA device 22. Now also referring to FIGS. 8 and 8*a*, in lieu of a wired connection, the camera module 10' communicates with the PDA 22 by a transceiver radio element 91 which is mounted in the proximal end of the module 10'. Similarly, the PDA 22 also includes its own transceiver radio module 85 which allows video signals transmitted by transceiver 91 to be received and then passed on to the video processor board 50 for further video signal processing, as necessary. Antennae 93 communicates with transceiver module 85 for enhancing reception of incoming video signals from the camera module 10'. The camera module 10' also has its own antennae 81 which enhances reception for authenticating signals which may be transmitted by transceiver 91. As understood by those skilled in the art, Bluetooth and other RF standards involve two-way communications whereby transmissions are authenticated and synchronized. Thus the transceiver module 85 whose main function is to receive a signal from the camera module 10', also transmits some signals to the camera module 10'. Accordingly, the camera module also acts as a receiver to authenticate and receive such signals. The proximal end of the camera module 10' also includes a rechargeable battery 79 which is recharged when the module 10' is seated within the opening 35 of the PDA 22. The battery 79 can be a common rechargeable nickel-cadmium or lithium-ion type battery. The battery 79 has a contact 77 protruding from the proximal tip of the camera module 10'. The deepest portion of chamber/opening 35 also has a contact 87 (shown schematically in FIG. 8) which makes contact with contact 77 when the camera module 10' is placed in the chamber. Contact 87 electrically couples with camera battery charging circuit 95 which provides an electrical charge for recharging the battery 79. When the camera module 10' is placed in the chamber 35, the external housing or casing of the camera module 10' is electrically conductive and contacts a ground (not shown) such as spring loaded clip within the chamber 35. Thus, recharge of the battery 79 can be accomplished.

As shown in FIG. 8, the charge circuit 95 receives power from power supply board 64. Thus, the battery 62 of the PDA also provides recharging capability to the battery 79.

The operation of the PDA is essentially the same in the second embodiment. If the user desires to transmit video images to another party, the user would grasp the camera module 10', remove it from chamber 35, and then point it at the target. The camera module 10' collects the video images through the objective lens group 18 which conditions images received by the image sensor 40. The plurality of conductors housed in the shielded miniature cable 21 transfers the video signals to the transceiver radio element 91. The transceiver radio element 91, among other functions, adds a high frequency carrier signal and base band protocol to the video signal which is then transmitted to the transceiver radio module 85. The video signal transmitted by the transceiver radio element 91 is authenticated by the transceiver radio module 85, the video signal is stripped of its carrier, and then routed by a link controller (not shown as a separate element apart from transceiver 85) to the video processor circuitry 50. The video signal is then handled in the same manner as the first embodiment. The user would depress the video switch 37 to initiate transmission of the video to the other party of the telephone call. Once the camera module 10' is removed from its seated position in the chamber 35, the contact between contacts 77 and 87 is broken. This break in electrical contact would allow the battery 79 to energize the camera module 10', and thus allow the camera module 10' to begin wirelessly communicating with the transceiver radio module 85 . The user would be able to easily hold and point the camera module 10' with one hand, while operating the PDA 22 in the other hand. As with the first embodiment, the video monitor 26 would display the video images simultaneously while video images were being transmitted to the other party so long as video switch 37 was depressed. If the user wished to receive video images transmitted from the other party, the user would simply reset the video switch 37 to its off or inactive state. The camera module 10' would continue to shoot video and communicate with the module 85; however, the video images would not be seen on screen 26. Again as with the first embodiment, a remote video device 60 could receive video images and remotely display and record the same.

Although FIG. 8 illustrates the video processor board 50 located within the PDA 22, the video processor board 50 may alternatively be co-located with the imaging device 40 within the distal tip of the camera module 10'. Accordingly, all necessary aid video processing may take place within the camera module and the video signal which would be transmitted by the radio transceiver element 91 is a post video signal which is ready for viewing by either the video monitor 26, or the remote video device 60 once the transceiver radio module 85 receives, authenticates, and strips the video signal of its carrier frequency as transmitted by the radio transceiver element 91.

FIG. 9 is a schematic diagram illustrating one way in which the imaging device 11 may be constructed. As illustrated, the image sensor 40 may include the timing and control circuits on the same planar structure. Power is supplied to image sensor 40 by power supply board 64. The connection between image sensor 40 and board 64 may simply be a cable having two conductors therein, one for ground and another for transmitting the desired voltage. These are illustrated as conductors 44 and 46. The output from image sensor 40 in the form of the pre-video signal is input to video processor board 50 by means of the conductor 48. In the configuration of FIG. 7, conductor 48 may simply be a 50-ohm conductor. Power and ground also are supplied to video processing board 50 by conductors 44 and 46 from power supply board 52. The output signal from the video processor board 50 is in the form of the post-video signal and which may be carried by conductor 49 which can also be a 50 ohm conductor. As discussed above with respect to the second embodiment, in lieu of a hard wired connection by conductors 48 and 49, the pre-video or post-video signal is transmitted wirelessly to the transceiver radio module 85.

Although FIG. 9 illustrates the image sensor and the timing and control circuits being placed on the same circuit board or planar structure, it is possible to separate the timing and control circuits from the pixel array and place the timing and control circuits onto video processing board 50. The advantage in placing the timing and control circuits on the same planar structure as the image sensor is that only three connections are required between image sensor 40 and the rest of the imaging device, namely, conductors 44, 46 and 48. Additionally, placing the timing and control circuits on the same planar structure with the pixel array results in the pre-video signal having less noise. Furthermore, the addition of the timing and control circuits to the same planar structure carrying the image sensor only adds a negligible amount of size to one dimension of the planar structure. If the pixel array is to be the only element on the planar structure, then additional connections must be made between the planar structure and the video processing board 50 in order to transmit the clock signals and other control signals to the pixel array. For example, a ribbon-type cable (not shown) or a plurality of 50-ohm coaxial cables (not shown) must be

used in order to control the downloading of information from the pixel array. Each of these additional connections would be hard wired between the boards.

FIG. **9***a* is a more detailed schematic diagram of image sensor **40** which contains an array of pixels **90** and the timing and control circuits **92**. One example of a pixel array **90** which can be used within the invention is similar to that which is disclosed in U.S. Pat. No. 5,471,515 to Fossum, et al., said patent being incorporated by reference herein. More specifically, FIG. 3 of Fossum, et al. illustrates the circuitry that makes up each pixel in the array of pixels **90**. The array of pixels **90** as described in Fossum, et al. is an active pixel group with intra-pixel charged transfer. The image sensor made by the array of pixels is formed as a monolithic complementary metal oxide semiconductor (CMOS) integrated circuit which may be manufactured in an industry standard complementary metal oxide semiconductor process. The integrated circuit includes a focal plane array of pixel cells, each one of the cells including a photo gate overlying the substrate for accumulating the photo generated charges. In broader terms, as well understood by those skilled in the art, an image impinges upon the array of pixels, the image being in the form of photons which strike the photo diodes in the array of pixels. The photo diodes or photo detectors convert the photons into electrical energy or electrons which are stored in capacitors found in each pixel circuit. Each pixel circuit has its own amplifier which is controlled by the timing and control circuitry discussed below. The information or electrons stored in the capacitors is unloaded in the desired sequence and at a desired frequency, and then sent to the video processing board **50** for further processing.

Although the active pixel array disclosed in U.S. Pat. No. 5,471,515 is mentioned herein, it will be understood that the hybrid CCD/CMOS described above, or any other solid state imaging device may be used wherein timing and control circuits can be placed either on the same circuit board or planar structure with the pixel array, or may be separated and placed remotely. Furthermore, it will be clearly understood that the invention claimed herein is not specifically limited to an image sensor as disclosed in the U.S. Pat. No. 5,471,515, but encompasses any image sensor which may be configured for use in conjunction with the other processing circuitry which makes up the imaging device of this invention.

To summarize the different options available in terms of arrangement of the components of the imaging device **11**, the array of pixels **90** of the image sensor **40** may be placed alone on a first plane, or the timing and control circuitry **92** may be placed with the array of pixels **90** on the first plane. If the timing and control circuitry **92** is not placed with the array of pixels **90** on the first plane, the timing and control circuitry **92** may be placed by itself on a second plane, or the timing and control circuitry **92** may be placed on a second plane with some or all of the processing circuitry from video processing board **50**. The video processing board **50** itself may be placed on one or more planes on corresponding circuit boards containing video processing circuitry. FIG. **1***a* illustrates a single video processor board **50** located directly behind image sensor **40**; however, it shall be understood that additional circuit boards containing additional circuitry may be placed behind the image sensor **40** and behind the video processing board **50**. Some or all of the video processing circuitry may be placed within the camera module **10** near the distal end thereof adjacent the image sensor **40**. Video processing circuitry which is not placed within the distal end of the camera module **10** may be placed within the housing **24** of the PDA. If video processing circuitry is placed near the distal end of the camera module **10**, it is preferable to arrange the video processing circuitry in a stacked relationship behind the image sensor **40**. Additionally, it is preferable to place the processing circuitry in a parallel arrangement with respect to image sensor **40** and to center such video processing circuitry along axis X-X in order to minimize the size of camera module **10**.

The timing and control circuits **92** are used to control the release of the image information or image signal stored in the pixel array. In the image sensor of Fossum, et al., the pixels are arranged in a plurality of rows and columns. The image information from each of the pixels is first consolidated in a row by row fashion, and is then downloaded from one or more columns that contain the consolidated information from the rows. As shown in FIG. **9***a*, the control of information consolidated from the rows is achieved by latches **94**, counter **96**, and decoder **98**. The operation of the latches, counter and decoder is similar to the operation of similar control circuitry found in other imaging devices. That is, a latch is a means of controlling the flow of electrons from each individual addressed pixel in the array of pixels. When a latch **94** is enabled, it will allow the transfer of electrons to the decoder **98**. The counter **96** is programmed to count a discrete amount of information based upon a clock input from the timing and control circuits **92**. When the counter **96** has reached its set point or overflows, the image information is allowed to pass through the latches **94** and be sent to the decoder **98** which places the consolidated information in a serial format. Once the decoder **98** has decoded the information and placed it in the serial format, then the row driver **100** accounts for the serial information from each row and enables each row to be downloaded by the column or columns. In short, the latches **94** will initially allow the information stored in each pixel to be accessed. The counter **96** then controls the amount of information flow based upon a desired time sequence. Once the counter has reached its set point, the decoder **98** then knows to take the information and place it in the serial format. The whole process is repeated, based upon the timing sequence that is programmed. When the row driver **100** has accounted for each of the rows, the row driver reads out each of the rows at the desired video rate.

The information released from the column or columns is also controlled by a series of latches **102**, a counter **104** and a decoder **106**. As with the information from the rows, the column information is also placed in a serial format which may then be sent to the video processing board **50**. This serial format of column information is the pre-video signal carried by conductor **48**. The column signal conditioner **108** places the column serial information in a manageable format in the form of desired voltage levels. In other words, the column signal conditioner **108** only accepts desired voltages from the downloaded column(s).

The clock input to the timing and control circuits **92** may simply be a quartz crystal timer. This clock input is divided into many other frequencies for use by the various counters. The run input to the timing and control circuit **92** may simply be an on/off control. The default input can allow one to input the pre-video signal to a video processor board which may run at a frequency of other than 30 hertz. The data input controls functions such as zoom. At least for a CMOS type active pixel array which can be accessed in a random manner, features such as zoom are easily manipulated by addressing only those pixels which locate a desired area of interest by the user.

A further discussion of the timing and control circuitry which may be used in conjunction with an active pixel array is disclosed in U.S. Pat. No. 5,471,515 and is also described in an article entitled "Active Pixel Image Sensor Integrated With Readout Circuits" appearing in *NASA Tech Briefs*, October 1996, pp. 38 and 39. This particular article is also incorporated by reference.

Once image sensor **40** has created the pre-video signal, it is sent to the video processing board **50** for further processing. At board **50**, as shown in FIG. **9***b*, the pre-video signal is passed through a series of filters. One common filter arrangement may include two low pass filters **114** and **116**, and a band pass filter **112**. The band pass filter only passes low frequency components of the signal. Once these low frequency components pass, they are then sent to detector **120** and white balance circuit **124**, the white balance circuit distinguishing between the colors of red and blue. The white balance circuit helps the imaging device set its normal, which is white. The portion of the signal passing through low pass filter **114** then travels through gain control **118** which reduces the magnitude or amplitude of this portion to a manageable level. The output from gain control **118** is then fed back to the white balance circuit **124**. The portion of the signal traveling through filter **116** is placed through the processor **122**. In the processor **122**, the portion of the signal carrying the luminance or non-chroma is separated and sent to the Y chroma mixer **132**. Any chroma portion of the signal is held in processor **122**.

Referring to the output of the white balance circuit **124**, this chroma portion of the signal is sent to a delay line **126** where the signal is then further reduced by switch **128**. The output of switch **128** is sent through a balanced modulator **130** and also to the Y chroma mixer **132** where the processed chroma portion of the signal is mixed with the processed non-chroma portion. Finally, the output from the Y chroma mixer **132** is sent to the NTSC/PAL encoder **134**, commonly known in the art as a "composite" encoder. The composite frequencies are added to the signal leaving the Y chroma mixer **132** in encoder **134** to produce the post-video signal which may be accepted by a television. Additionally, the signal from Y chroma mixer **132** is sent to the digital signal processor **72** so those images can be viewed on monitor **26**.

In addition to the functions described above that are achieved by the digital signal processor **72**, the processor **72** can also provide additional digital enhancements. Specifically, digital enhancement can sharpen or otherwise clarify the edges of an image viewed on a video screen which might normally be somewhat distorted. Additionally, selected background or foreground images may be removed thus only leaving the desired group of images.

In addition to digital enhancement, the digital signal processor **72** can include other circuitry that may further condition the signal received from board **50** so that it may be viewed in a desired format other than NTSC/PAL. One common encoder which can be used would be an RGB encoder. An RGB encoder separates the signal into the three primary colors (red, green and blue). A SVHS encoder (super video home system) encoder could also be added to processor **72**. This type of encoder splits or separates the luminance portion of the signal and the chroma portion of the signal. Some observers believe that a more clear signal is input to the video device by such a separation, which in turn results in a more clear video image viewed on the video device. Another example of an encoder which could be added to processor **72** includes a VGA compatible encoder, which enables the video signal to be viewed on a standard VGA monitor which is common to many computer monitors.

One difference between the arrangement of image sensor **40** and the outputs found in FIG. 3 of the Fossum, et al. patent is that in lieu of providing two analog outputs [namely, VS out (signal) and VR out (reset)], the reset function takes place in the timing and control circuitry **92**. Accordingly, the pre-video signal only requires one conductor **48**.

FIGS. **10***a*–**10***e* illustrate in more detail one example of circuitry which may be used in the video processing board **50** in order to produce a post-video signal which may be directly accepted by a NTSC/PAL compatible video device such as a television. The circuitry disclosed in FIGS. **10***a*–**10***e* is very similar to circuitry that is found in a miniature quarter-inch Panasonic camera, Model KS-162. It will be understood by those skilled in the art that the particular arrangement of elements found in FIGS. **10***a*–**10***e* are only exemplary of the type of video processing circuitry which may be incorporated in order to take the pre-video signal and condition it to be received by a desired video device.

As shown in FIG. **10***a*, 5-volt power is provided along with a ground by conductors **44** and **46** to board **50**. The pre-video signal carried by conductor **48** is buffered at buffer **137** and then is transferred to amplifying group **138**. Amplifying group **138** amplifies the signal to a usable level as well as achieving impedance matching for the remaining circuitry.

The next major element is the automatic gain control **140** shown in FIG. **10***b*. Automatic gain control **140** automatically controls the signal from amplifying group **138** to an acceptable level and also adds other characteristics to the signal as discussed below. More specifically, automatic gain control **140** conditions the signal based upon inputs from a 12-channel digital to analog converter **141**. Converter **141** retrieves stored information from EEPROM (electrically erasable programmable read only memory) **143**. EEPROM **143** is a non-volatile memory element, which may store user information, for example, settings for color, tint, balance and the like. Thus, automatic gains controls **140** changes the texture or visual characteristics based upon user inputs. Housing **24** could also include buttons for controlling the image viewed on monitor **26** such as a gain control **140**. The signal leaving the automatic gain control **140** is an analog signal until being converted by analog to digital converter **142**.

Digital signal processor **144** of FIG. **10***c* further processes the converted signal into a serial type digital signal. One function of the microprocessor **146** is to control the manner in which digital signal processor **144** sorts the digital signals emanating from converter **142**. Microprocessor **146** also controls analog to digital converter **142** in terms of when it is activated, when it accepts data, when to release data, and the rate at which data should be released. Microprocessor **146** may also control other functions of the imaging device such as white balance. The microprocessor **146** may selectively receive the information stored in the EEPROM **143** and carry out its various commands to further control the other elements within the circuitry.

After the signal is processed by digital signal processor **144**, the signal is sent to digital encoder **148** illustrated in FIG. **10***d*. Some of the more important functions of digital encoder **148** are to encode the digital signal with synchronization, modulated chroma, blanking, horizontal drive, and the other components necessary so that the signal may be

placed in a condition for reception by a video device such as a television monitor. As also illustrated in FIG. **10***d*, once the signal has passed through digital encoder **148**, the signal is reconverted into an analog signal through digital to analog converter **150**.

This reconverted analog signal is then buffered at buffers **151** and then sent to amplifier group **152** of FIG. **10***e* which amplifies the signal so that it is readily accepted by a desired video device. Specifically, as shown in FIG. **10***e*, one SVHS outlet is provided at **160**, and two composite or NTSC outlets are provided at **162** and **164**, respectively.

From the foregoing, it is apparent that an entire imaging device may be incorporated within the distal tip of the camera module, or may have some elements of the imaging device being placed in the housing of the PDA. Based upon the type of image sensor used, the profile area of the imaging device may be made small enough to be placed into a camera module which has a very small diameter.

This invention has been described in detail with reference to particular embodiments thereof, but it will be understood that various other modifications can be effected within the spirit and scope of this invention.

What is claimed is:

1. In a PDA having capability to transmit and receive data in a communications network, the improvement comprising:

a video system integral with said PDA for receiving and transmitting video images, and for viewing said video images, said video system comprising;

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal, a first circuit board mounted in said camera module and electrically coupled to said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format, said camera module further including a transceiver radio element mounted therein and electrically communicating with said first circuit board to transmit the converted pre-video signal;

a transceiver radio module mounted in said PDA for wirelessly communicating with said transceiver element in said camera module to receive said converted pre-video signal;

a video view screen attached to said PDA for viewing said video images, said video view screen communicating with said transceiver radio module for displaying video images processed by said first circuit board.

2. A device, as claimed in claim **1**, wherein:

said image sensor defines a profile area in said first plane, and said first circuit board is positioned in longitudinal alignment with said image sensor such that said first circuit board does not extend substantially beyond said profile.

3. A device, as claimed in claim **1**, further including:

a second circuit board electrically coupled with said first circuit board and said image sensor for further processing said pre-video signal, said second board being placed adjacent said first circuit board within said camera module.

4. A device, as claimed in claim **1**, wherein:

said first and second planes are offset from and substantially parallel to one another.

5. A device, as claimed in claim **3**, wherein:

said second circuit board lies in a third plane which is offset from and extends substantially parallel to said first and second planes.

6. A device, as claimed in claim **3**, wherein:

said second circuit board includes means for digital signal processing enabling the pre-video signal conditioned by said first circuit board to be viewed by said video view screen.

7. A device, as claimed in claim **1**, wherein:

said first circuit board converts said pre-video signal to a post-video signal for direct reception by a remote video device, said post-video signal being of a format selected from the group consisting of a NTSC/PAL video signal and a VGA video signal.

8. A device, as claimed in claim **1**, wherein:

said pixels are CMOS pixels.

9. A device, as claimed in claim **1**, wherein:

said transceiver radio element and said transceiver radio module communicate by a bluetooth communications standard.

10. A device, as claimed in claim **1**, wherein:

said transceiver radio module and said transceiver radio element communicate by an IEEE 802.15.13 communications standard.

11. A device, as claimed in claim **1**, wherein:

said array of pixels includes an array of passive CMOS pixels, wherein individual passive CMOS pixels of said array of passive CMOS pixels each include a photo diode for producing photoelectrically generated signals, and an access transistor communicating with said photo diode to control the release of photoelectrically generated signals.

12. A device, as claimed in claim **1**, wherein:

individual pixels within said array of pixels each include an amplifier.

13. A device, as claimed in claim **1**, wherein:

said PDA includes a text screen mounted therein for viewing text which is manipulated by a user.

14. A device as claimed in claim **1**, further including:

a wireless telephone attached to said PDA.

15. A device, as claimed in claim **1**, further including:

a remote video device electrically coupled to said video system for further viewing said video images.

16. A device, as claimed in claim **15**, wherein:

said remote video device is selected from the group consisting of a television and a computer monitor.

17. A device, as claimed in claim **1** wherein:

said PDA further includes a camera battery charge circuit mounted therein for recharging said camera module, said camera module having an integral source of power which electrically communicates with said charge circuit when said camera module is mounted in said PDA.

18. In a PDA having capability to transmit and receive data in a communications network, the improvement comprising:

a video system integral with said PDA for receiving and transmitting video images, and for viewing said video images, said video system comprising;

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal, said camera module further including a transceiver radio element

mounted therein and electrically communicating with said circuitry means to transmit the pre-video signal to the PDA;

a transceiver radio module mounted in said PDA for wirelessly communicating with said transceiver element in said camera module to receive said pre-video signal;

a first circuit board mounted in said PDA and electrically communicating with said transceiver radio module for converting said pre-video signal into a desired video format;

a video view screen attached to said PDA for viewing said video images, said video view screen communicating with said first circuit board for displaying video images processed by said first circuit board.

19. A device, as claimed in claim **18**, wherein:

said pixels are CMOS pixels.

20. A device, as claimed in claim **18**, wherein:

said transceiver radio element and said transceiver radio module communicate by a bluetooth communications standard.

21. A device, as claimed in claim **18**, wherein:

said transceiver radio module and said transceiver radio element communicate by an IEEE 802.15.13 communications standard.

22. In a PDA having capability to transmit and receive data in a communications network, the PDA having a housing, and a video view screen for viewing the data which includes video signals, the improvement comprising:

a camera module for taking video images, said camera module communicating with circuitry within said PDA enabling viewing on said video view screen and enabling video signals to be transmitted from said camera module to said computer, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of said pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal, a first circuit board electrically connected to said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;

a transceiver radio element housed within said camera module and electrically coupled to said first circuit board for transmitting said converted pre-video signal; and

a transceiver radio module housed in the PDA and wirelessly communicating with said transceiver radio element for receiving said converted pre-video signal, and said transceiver radio element being electrically coupled to the video view screen of the PDA enabling viewing of the converted pre-video signals.

23. A device, as claimed in claim **22**, wherein:

said pixels are CMOS pixels.

24. A device, as claimed in claim **22**, wherein:

said transceiver radio element and said transceiver radio module communicate by a bluetooth communications standard.

25. A device, as claimed in claim **22**, wherein:

said transceiver radio module and said transceiver radio element communicate by an IEEE 802.15.13 communications standard.

26. A device, as claimed in claim **22** wherein:

said PDA further includes a camera battery charge circuit mounted therein for recharging said camera module, said camera module having an integral source of power which electrically communicates with said charge circuit when said camera module is mounted in said PDA.

27. In a PDA having capability to transmit data between a computer connected to a communications network, the PDA having a housing, and a video view screen for viewing the data which includes video signals, the improvement comprising:

a camera module for taking video images, said camera module communicating with circuitry within said PDA enabling viewing on said video view screen and enabling video signals to be transmitted from said camera module to said computer, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of said pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal;

a transceiver radio element housed within said camera module and electrically coupled to said image sensor for transmitting said pre-video signal;

a transceiver radio module housed in the PDA and wirelessly communicating with said transceiver radio element for receiving said pre-video signal; and

a first circuit board housed within the PDA and electrically coupled to said transceiver radio module for taking said pre video signal and conditioning it to be a post video signal in a desired format, and said transceiver radio element being electrically coupled to the video view screen of the PDA enabling viewing of the converted pre-video signals.

28. A device, as claimed in claim **27**, wherein:

said pixels are CMOS pixels.

29. A device, as claimed in claim **27**, wherein:

said transceiver radio element and said transceiver radio module communicate by a bluetooth communications standard.

30. A device, as claimed in claim **27**, wherein:

said transceiver radio module and said transceiver radio element communicate by an IEEE 802.15.13 communications standard.

31. A device, as claimed in claim **27** wherein:

said PDA further includes a camera battery charge circuit mounted therein for recharging said camera module, said camera module having an integral source of power which electrically communicates with said charge circuit when said camera module is mounted in said PDA.

32. A PDA having capability to transmit and receive data in a communications network, said PDA comprising:

an image sensor lying in a first plane, and an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal;

a first circuit board electrically communicating with said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;

a camera module housing said image sensor and said first circuit board;

a transceiver radio element mounted in said camera module communicating with said first circuit board for wirelessly transmitting the converted pre-video signal;

a transceiver radio module communicating wirelessly with said transceiver radio element for receiving the converted pre-video signal;

a transceiver/amplifier section electrically coupled to said transceiver radio module for amplifying and further transmitting the converted pre-video signal, and for receiving, and amplifying video and audio signals transmitted by another party;

a digital signal processor electrically coupled to said transceiver radio module and said transceiver/amplifier section, said digital signal processor further conditioning said converted pre-video signal, and also for conditioning video and audio signals received by said transceiver/amplifier section from the other party;

a microphone electrically communicating with said digital signal processor for recording sound and converting the sound to audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting the audio signals;

a video view screen attached to said PDA, said video view screen for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section from the other party;

a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video view screen; and

a PDA power supply mounted in said PDA for providing power thereto.

33. A device, as claimed in claim **32**, wherein:

said pixels are CMOS pixels.

34. A device, as claimed in claim **32**, wherein:

said transceiver radio element and said transceiver radio module communicate by a bluetooth communications standard.

35. A device, as claimed in claim **32**, wherein:

said transceiver radio module and said transceiver radio element communicate by an IEEE 802.15.13 communications standard.

36. A device, as claimed in claim **32** wherein:

said PDA further includes a camera battery charge circuit mounted therein for recharging said camera module, and said camera module further includes a camera module source of power mounted in said camera module which electrically communicates with said charge circuit when said camera module is mounted in said PDA.

37. A PDA having capability to transmit and receive data in a communications network, said PDA comprising:

an image sensor lying in a first plane, and an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal;

a camera module housing said image sensor;

a transceiver radio element mounted in said camera module communicating with said image sensor for wirelessly transmitting the pre-video signal;

a transceiver radio module communicating wirelessly with said transceiver radio element for receiving the pre-video signal;

a first circuit board electrically communicating with said transceiver radio module, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;

a transceiver/amplifier section electrically coupled to said transceiver radio module for amplifying and further transmitting the converted pre-video signal, and for receiving, and amplifying video and audio signals transmitted by another party;

a digital signal processor electrically coupled to said transceiver radio module and said transceiver/amplifier section, said digital signal processor further conditioning said converted pre-video signal, and also for conditioning video and audio signals received by said transceiver/amplifier section from the other party;

a microphone electrically communicating with said digital signal processor for recording sound and converting the sound to audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting the audio signals;

a video view screen attached to said PDA, said video view screen for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section from the other party;

a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video view screen; and

a PDA power supply mounted in said PDA for providing power thereto.

38. A device, as claimed in claim **37**, wherein:

said pixels are CMOS pixels.

39. A device, as claimed in claim **37**, wherein:

said transceiver radio element and said transceiver radio module communicate by a bluetooth communications standard.

40. A device, as claimed in claim **37**, wherein:

said transceiver radio module and said transceiver radio element communicate by an IEEE 802.15.13 communications standard.

41. A device, as claimed in claim **37** wherein:

said PDA further includes a camera battery charge circuit mounted therein for recharging said camera module, and said camera module further includes a camera module source of power mounted in said camera module which electrically communicates with said charge circuit when said camera module is mounted in said PDA.

42. In a PDA having capability to transmit and receive data in a communications network, the improvement comprising:

a video system integral with said PDA for receiving and transmitting video images, and for viewing said images, said video system comprising:

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically coupled to said image sensor, said first circuit board including circuitry means for timing and control of said array of pixels and circuitry means for processing and converting said pre-video signal to a desired video format, a transceiver radio element communicating with said firs circuit board for transmitting said converted pre-video signal;

a transceiver radio module mounted in said PDA for wirelessly receiving said converted pre-video signal; and

a video view screen attached to said PDA for viewing said video images, said video view screen communicating with said transceiver radio module, and displaying video images processed by said first circuit board.

43. A device, as claimed in claim **42**, wherein:

said pixels are CMOS pixels.

44. A device, as claimed in claim **42**, wherein:

said transceiver radio element and said transceiver radio module communicate by a bluetooth communications standard.

45. A device, as claimed in claim **42**, wherein:

said transceiver radio module and said transceiver radio element communicate by an IEEE 802.15.13 communications standard.

46. In a PDA having capability to transmit and receive data in a communications network, the improvement comprising:

a video system integral with said PDA for receiving and transmitting video images, and for viewing said images, said video system comprising:

a camera module housing an image sensor therein, said image sensor including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal, a transceiver radio element communicating with said image sensor for transmitting said pre-video signal;

a transceiver radio module mounted in said PDA for wirelessly receiving said pre-video signal;

a first circuit board electrically coupled to said transceiver radio module, said first circuit board including circuitry means for timing and control of said array of pixels and circuitry means for processing and converting said pre-video signal to a desired video format, and

a video view screen attached to said PDA for viewing said video images, said video view screen communicating with said transceiver radio module, and displaying video images processed by said first circuit board.

47. A device, as claimed in claim **46**, wherein:

said pixels are CMOS pixels.

48. A device, as claimed in claim **46**, wherein:

said transceiver radio element and said transceiver radio module communicate by a bluetooth communications standard.

49. A device, as claimed in claim **46**, wherein:

said transceiver radio module and said transceiver radio element communicate by an IEEE 802.15.13 communications standard.

50. In a PDA having capability to transmit and receive data in a communications network, the PDA including a video view screen for viewing video images, the improvement comprising:

a camera module for taking video images, said camera module wirelessly communicating with circuitry within said PDA enabling viewing on said video view screen and enabling video signals to be transmitted from said camera module to the personal computer, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically connected to said image sensor, said first circuit board including circuitry means for timing and control of said array of pixels and circuitry means for processing and converting said pre-video signal to a desired video format, and a transceiver radio element housed in the camera module for wirelessly transmitting the converted pre-video signal to the PDA.

51. A device, as claimed in claim **50**, wherein:

said pixels are CMOS pixels.

52. A device, as claimed in claim **50**, wherein:

said transceiver radio element communicates with the PDA by a bluetooth communications standard.

53. A device, as claimed in claim **50**, wherein:

said transceiver radio element communicates with the PDA by an IEEE 802.15.13 communications standard.

54. In a PDA having capability to transmit and receive data in a communications network, the PDA including a video view screen for viewing video images, the improvement comprising:

a camera module for taking video images, said camera module wirelessly communicating with circuitry within said PDA enabling viewing on said video view screen and enabling video signals to be transmitted from said camera module to the personal computer, said camera module including an image sensor housed therein, said image sensor including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal, and a transceiver radio element housed in the camera module for wirelessly transmitting the pre-video signal to the PDA.

55. A device, as claimed in claim **54**, wherein:

said pixels are CMOS pixels.

56. A device, as claimed in claim **54**, wherein:

said transceiver radio element communicates with the PDA by a bluetooth communications standard.

57. A device, as claimed in claim **54**, wherein:

said transceiver radio element communicates with the PDA by an IEEE 802.15.13 communications standard.

58. In a PDA having capability to transmit and receive data in a communications network, the PDA including a video view screen for viewing the video images, the improvement comprising:

a camera module for taking video images, said camera module communicating with circuitry within said PDA enabling viewing of said video images on said PDA and enabling video signals to be transmitted from said camera module to the personal computer, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of said pixels for timing and control of said array of pixels, said circuitry means for timing and control placed remote from said array of pixels on a second plane, said image sensor producing a pre-video signal, a first circuit board electrically connected to said image sensor and lying in a third plane, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format, and a radio transceiver element communicating with said first circuit board for wirelessly transmitting said converted pre-video signal.

59. A device, as claimed in claim **58**, wherein:

said pixels are CMOS pixels.

60. A device, as claimed in claim **58**, wherein:

said transceiver radio element communicates with the PDA by a bluetooth communications standard.

61. A device, as claimed in claim **58**, wherein:

said transceiver radio element communicates with the PDA by an IEEE 802.15.13 communications standard.

62. In a PDA having capability to transmit and receive data in a communications network, the PDA including a video view screen for viewing the video images, the improvement comprising:

a camera module for taking video images, said camera module communicating with circuitry within said PDA enabling viewing of said video images on said PDA and enabling video signals to be transmitted from said camera module to the personal computer, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of said pixels for timing and control of said array of pixels, said circuitry means for timing and control placed remote from said array of pixels on a second plane, said image sensor producing a pre-video signal, and a radio transceiver element communicating with said image sensor for wirelessly transmitting said pre-video signal.

63. A device, as claimed in claim 62, wherein:

said pixels are CMOS pixels.

64. A device, as claimed in claim 62, wherein:

said transceiver radio element communicates with the PDA by a bluetooth communications standard.

65. A device, as claimed in claim 62, wherein:

said transceiver radio element communicates with the PDA by an IEEE 802.15.13 communications standard.

66. A PDA having capability to transmit and receive data in a communications network, said PDA comprising:

an image sensor lying in a first plane including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal;

a first circuit board electrically communicating with said image sensor, said first circuit board including circuitry means for timing and control of said array of pixels and circuitry means for processing and converting said pre-video signal to a desired video format;

a radio transceiver element communicating with said first circuit board for wirelessly transmitting said converted pre-video signal;

a camera module housing said image sensor, said first circuit board, and said transceiver radio element therein;

a radio transceiver module housed within the PDA for wirelessly communicating with said radio transceiver element and receiving said converted pre-video signal;

a transceiver/amplifier section electrically coupled to said transceiver radio module for amplifying and further transmitting the converted pre-video signal, and for receiving, and amplifying video and audio signals transmitted by another party;

a digital signal processor electrically coupled to said transceiver radio module and said transceiver/amplifier section, said digital signal processor further conditioning said pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals received by said transceiver/amplifier section from the other party;

a microphone electrically communicating with said digital signal processor for receiving sound and converting the sound to audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video view screen attached to said PDA, said video view screen for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section; and

a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video view screen; and

a power supply mounted to said PDA for providing power thereto.

67. A device, as claimed in claim 66, wherein:

said pixels are CMOS pixels.

68. A device, as claimed in claim 66, wherein:

said transceiver radio element and said transceiver radio module communicate by a bluetooth communications standard.

69. A device, as claimed in claim 66, wherein:

said transceiver radio module and said transceiver radio element communicate by an IEEE 802.15.13 communications standard.

70. A PDA having capability to transmit and receive data in a communications network, said PDA comprising:

an image sensor lying in a first plane including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal;

a first circuit board electrically communicating with said image sensor, said first circuit board including circuitry means for timing and control of said array of pixels; a radio transceiver element communicating with said first circuit board for wirelessly transmitting said pre-video signal;

a camera module housing said image sensor, said first circuit board, and said transceiver radio element therein;

a radio transceiver module housed within the PDA for wirelessly communicating with said radio transceiver element and receiving said pre-video signal;

a second circuit board electronically communicating with said radio transceiver module, said second circuit board including circuitry means for converting said pre-video signal to a desired video format;

a transceiver/amplifier section electrically coupled to said transceiver radio module for amplifying and further transmitting the converted pre-video signal, and for receiving, and amplifying video and audio signals transmitted by another party;

a digital signal processor electrically coupled to said transceiver radio module and said transceiver/amplifier section, said digital signal processor further conditioning said pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals received by said transceiver/amplifier section from the other party;

a microphone electrically communicating with said digital signal processor for receiving sound and converting the sound to audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video view screen attached to said PDA, said video view screen for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section;

a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video view screen; and

a power supply mounted to said PDA for providing power thereto.

71. A device, as claimed in claim 70, wherein:
said pixels are CMOS pixels.

72. A device, as claimed in claim 70, wherein:
said transceiver radio element and said transceiver radio module communicate by a bluetooth communications standard.

73. A device, as claimed in claim 70, wherein:
said transceiver radio module and said transceiver radio element communicate by an IEEE 802.15.13 communications standard.

74. A PDA having capability to transmit and receive data in a communications network, said PDA comprising:
an image sensor lying in a first plane, and an array of pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of pixels for timing and control of said array of pixels, said circuitry means for timing and control being placed remote from said array of pixels on a second plane, said image sensor producing a pre-video signal;
a first circuit board electrically coupled with said image sensor and lying in a third plane, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format;
a transceiver radio element communicating with said first circuit board to wirelessly transmit the converted pre-video signal;
a camera module housing said image sensor, said first circuit board and said transceiver radio element;
a transceiver/amplifier section electrically coupled to said transceiver radio module for amplifying and further transmitting said converted pre-video signal and for receiving and amplifying video and audio signals transmitted by another party;
a digital signal processor electrically coupled to said transceiver radio module and said transceiver/amplifier section, said digital signal processor further conditioning said converted pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals received by said transceiver/amplifier section from the other party;
a microphone electrically communicating with said digital signal processor for receiving sound and converting the sound to audio signals;
a speaker electrically communicating with said digital signal processor for broadcasting audio signals;
a video view screen attached to said PDA, said video view screen for selectively displaying selectively displaying video images from said image device, and for selectively displaying video images received by said transceiver/amplifier section from the other party; and a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video view screen; and
a power supply mounted to said PDA for providing power thereto.

75. A device, as claimed in claim 74, wherein:
said pixels are CMOS pixels.

76. A device, as claimed in claim 74, wherein:
said transceiver radio element and said transceiver radio module communicate by a bluetooth communications standard.

77. A device, as claimed in claim 74, wherein:
said transceiver radio module and said transceiver radio element communicate by an IEEE 802.15.13 communications standard.

78. In a method for conducting video conferencing communications through a communications network, the improvement comprising the steps of:
providing a camera module having an image sensor housed therein;
removing the camera module from connection with the PDA;
pointing the camera module at a targeted object and taking video images of the targeted object;
wirelessly transmitting the video images taken by image sensor to the PDA;
processing the video images transmitted by the camera module; and
selectively viewing the video images on the PDA and selectively transmitting the video images to another party.

79. A method, as claimed in claim 78, wherein:
said image sensor includes a CMOS pixel array.

80. In a PDA having capability to transmit and receive data communications network, the improvement comprising:
a camera module housing an image sensor therein, said camera module for producing video images of a targeted object;
means for wirelessly interconnecting said camera module to said PDA, said means for wirelessly interconnecting enabling said camera module to be selectively displaced away from and not in contact with said PDA; and
a video view screen attached to said PDA for selectively viewing video images taken by said camera module, and for selectively viewing incoming video images received from the personal computer connected to the global communications network.

81. A device, as claimed in claim 80, wherein: said PDA includes a housing, and an opening for receiving said camera module so as to place said camera module in a stored position.

82. In a PDA having the capability to transmit data between a personal computer connected to a communications network, the improvement comprising:
a camera module housing an image sensor therein;
a camera module battery housed within said camera module for providing power to said camera module;
a camera battery charge circuit housed within the PDA;
a PDA battery housed within the PDA for providing power to said camera battery charge circuit; and
wherein the camera module is received in the PDA so said camera module battery electrically communicates with said camera battery charge circuit to selectively charge said camera module battery.

83. A method of powering and recharging a camera module for use with a PDA, said method comprising the steps of:
providing a PDA including a camera battery charge circuit and a PDA battery housed therein;
providing a camera module housing an image sensor therein for taking video images, and a camera module battery housed within said camera module for selectively powering said camera module;
removing said camera module from seated engagement with the PDA resulting in activation of said camera module battery for powering said camera module; and
returning said camera module to its seated position with said PDA and in electrical communication with the battery charge circuit to charge said camera module battery.

* * * * *

US006424369B1

(12) **United States Patent**
Adair et al.

(10) **Patent No.: US 6,424,369 B1**
(45) **Date of Patent: Jul. 23, 2002**

(54) **HAND-HELD COMPUTERS INCORPORATING REDUCED AREA IMAGING DEVICES**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 45 days.

(21) Appl. No.: **09/638,976**

(22) Filed: **Aug. 15, 2000**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/496,312, filed on Feb. 1, 2000, which is a continuation of application No. 09/175,685, filed on Oct. 20, 1998, now Pat. No. 6,043,839, which is a continuation-in-part of application No. 08/944,322, filed on Oct. 6, 1997, now Pat. No. 5,929,901.

(51) **Int. Cl.**[7] **H04N 7/18**

(52) **U.S. Cl.** **348/76**; 348/376; 455/566; 455/556

(58) **Field of Search** 348/76–80, 10–18, 348/69–75, 158, 373, 376; 455/556, 566, 346, 345

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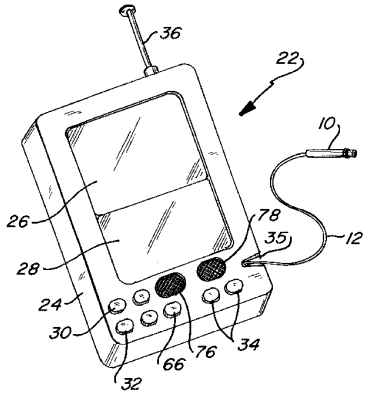
Primary Examiner—Andy Rao
(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

A reduced area imaging device is provided for use with a miniature hand-held computer referred to in the industry as a PDA. In one configuration of the imaging device, the image sensor is placed remote from the remaining image processing circuitry. In a second configuration, all of the image processing circuitry to include the image sensor is placed in a stacked fashion near the same location. In the first configuration, the entire imaging device can be placed at the distal end of a camera module. In a second configuration, the image sensor is remote from the remaining image processing circuitry wherein available space within the PDA is used to house the remaining circuitry. In any of the embodiments, the image sensor may be placed alone on a first circuit board, or timing and control circuits may be included on the first circuit board containing the image sensor. One or more video processing boards can be stacked in a longitudinal fashion with respect to the first board, or the video processing boards may be placed within the housing of the communication device. The PDA includes a miniature LCD-type video view screen which is capable of viewing not only the images taken by the camera module, but also can show incoming video images received from a personal computer connected to a global communications network. The camera module is of such small size that it can be easily stored within the housing of the PDA, and may be attached thereto as by a small retractable cable.

75 Claims, 12 Drawing Sheets



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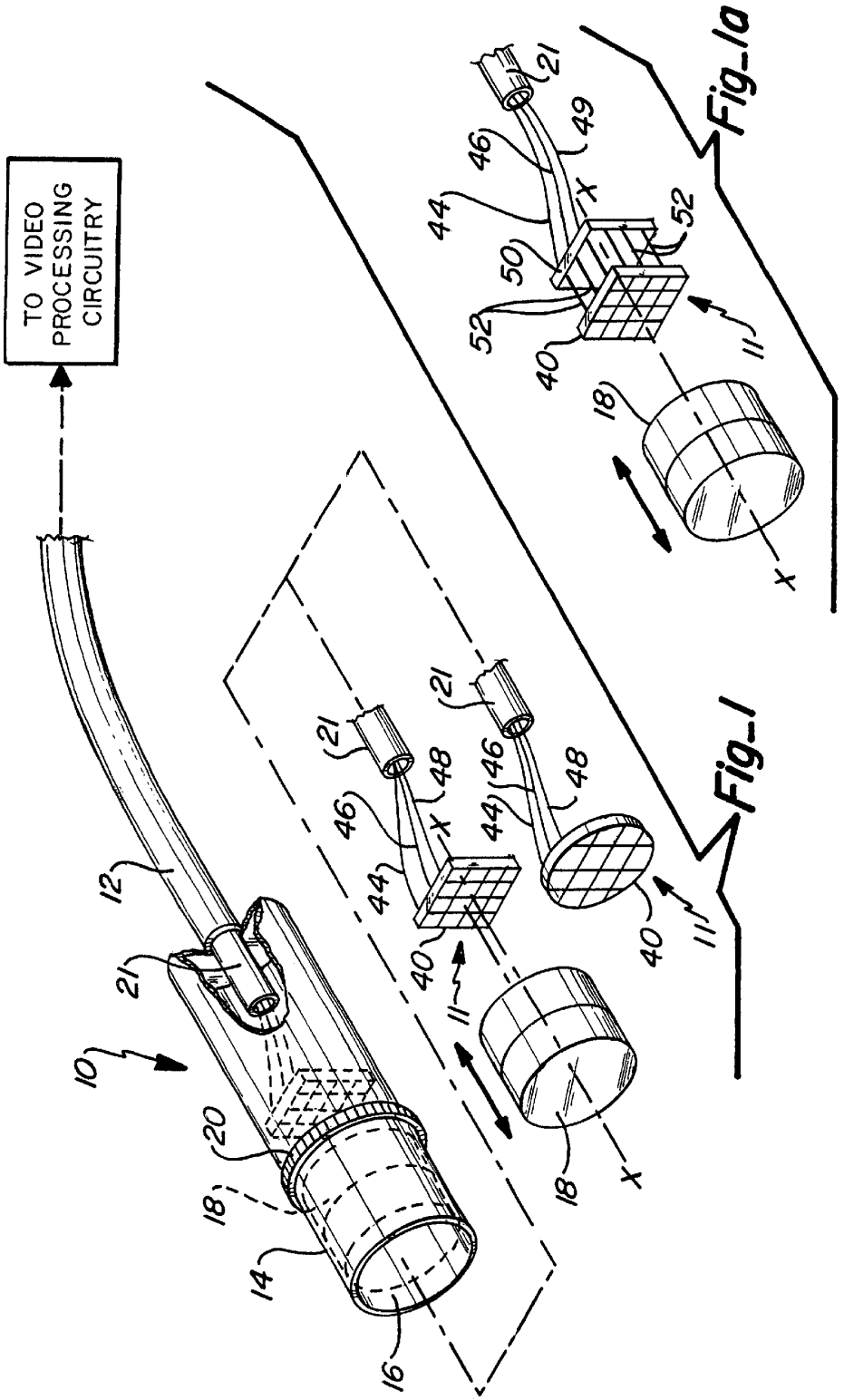
TO VIDEO PROCESSING CIRCUITRY
10
12
14
16
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48
49
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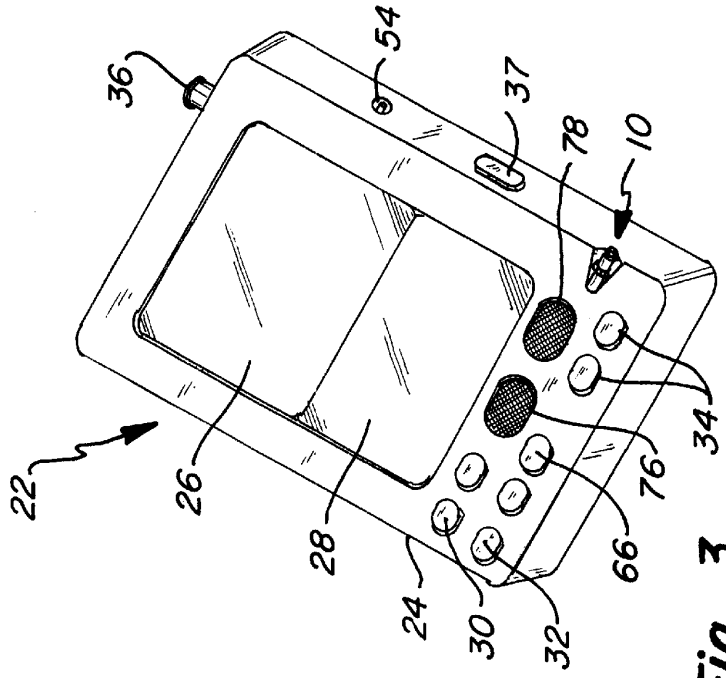
52
X
11

Fig_1a

Fig_1


36
54
37
78
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22
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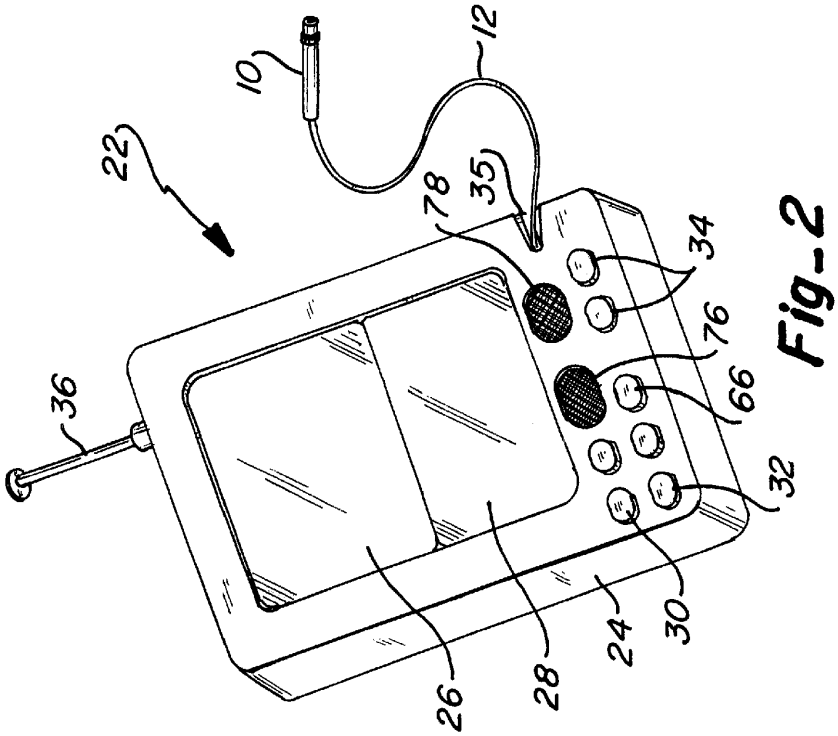
32
66
76
34

Fig_3


10
12
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78
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76
66
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28
24
30

Fig_2

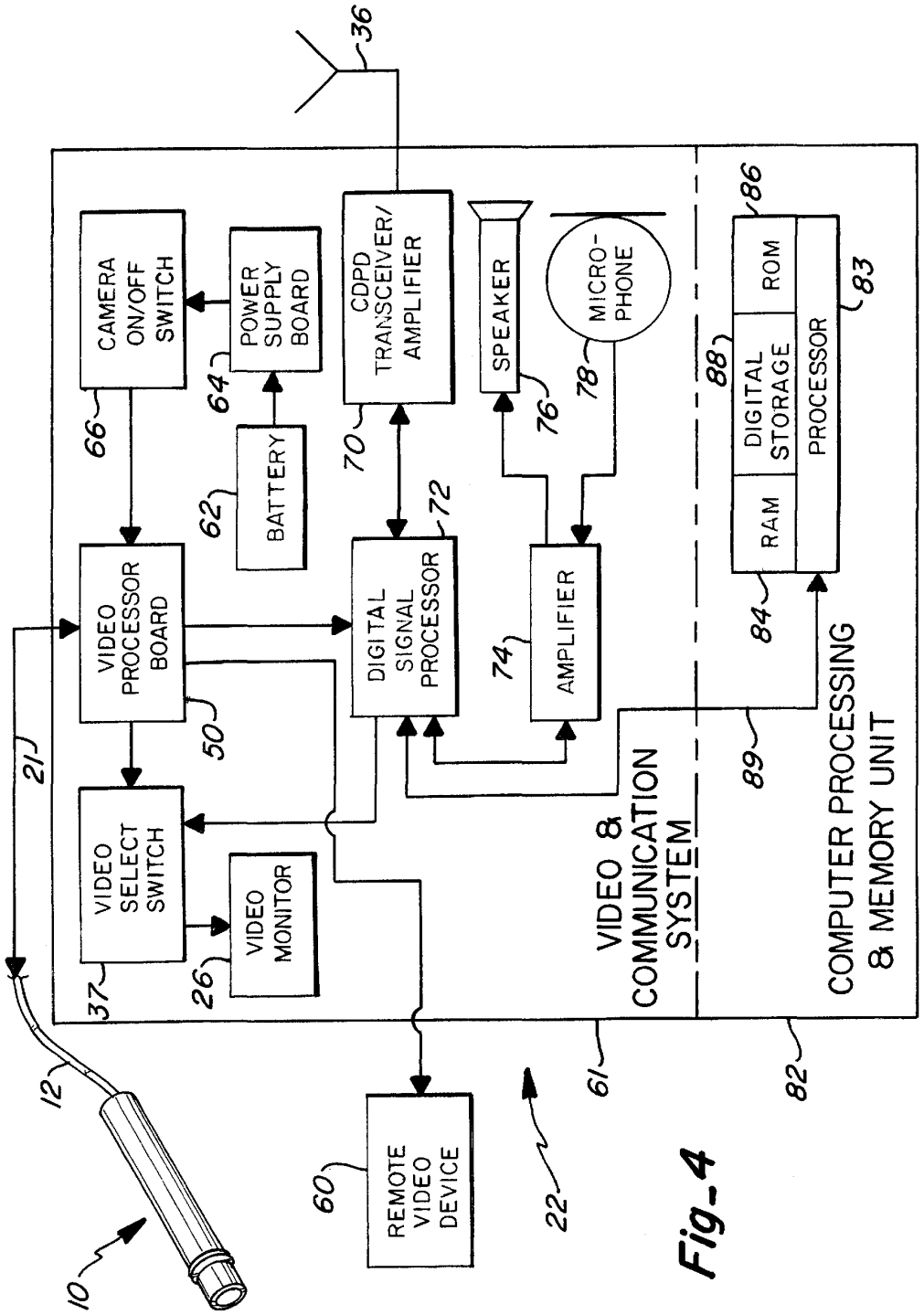

36
CAMERA ON/OFF SWITCH
POWER SUPPLY BOARD
CDPD TRANSCEIVER/ AMPLIFIER
SPEAKER
MICRO-PHONE
86
ROM
DIGITAL STORAGE
RAM
PROCESSOR
83
88
64
66
70
76
78
62
BATTERY
72
VIDEO PROCESSOR BOARD
DIGITAL SIGNAL PROCESSOR
AMPLIFIER
74
84
50
21
89
VIDEO SELECT SWITCH
VIDEO MONITOR
26
37
VIDEO & COMMUNICATION SYSTEM
COMPUTER PROCESSING & MEMORY UNIT
12
61
82
60
REMOTE VIDEO DEVICE
22
10

Fig_4

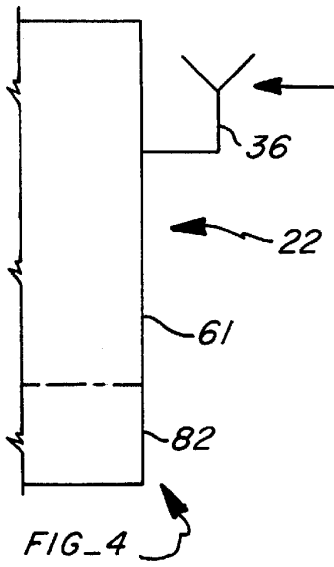


FIG_4

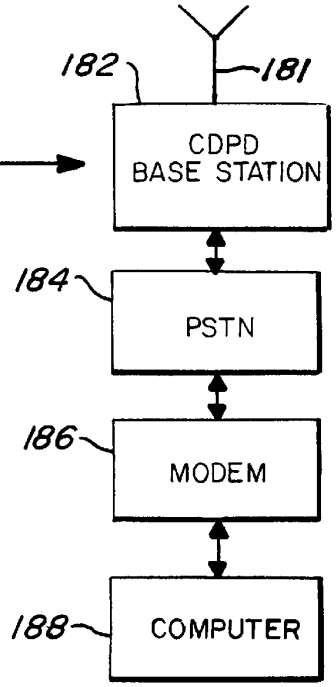


Fig_5

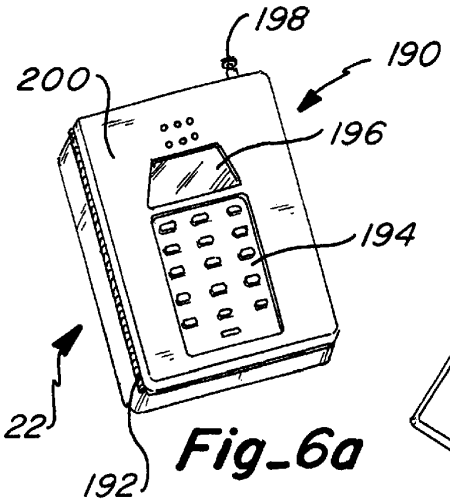


Fig_6a

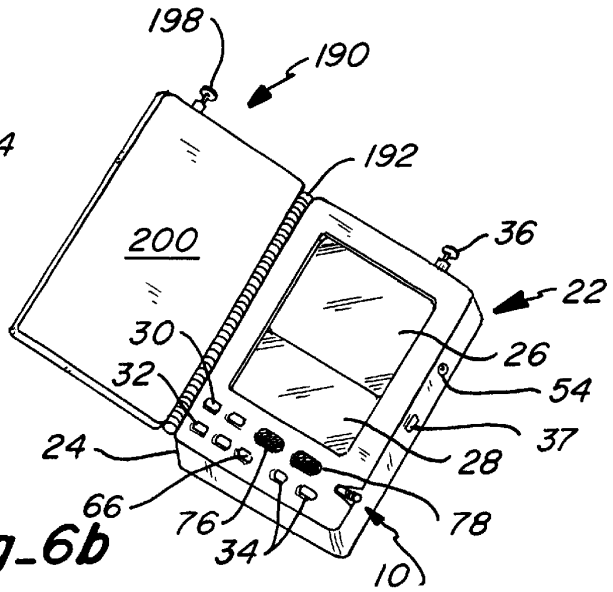
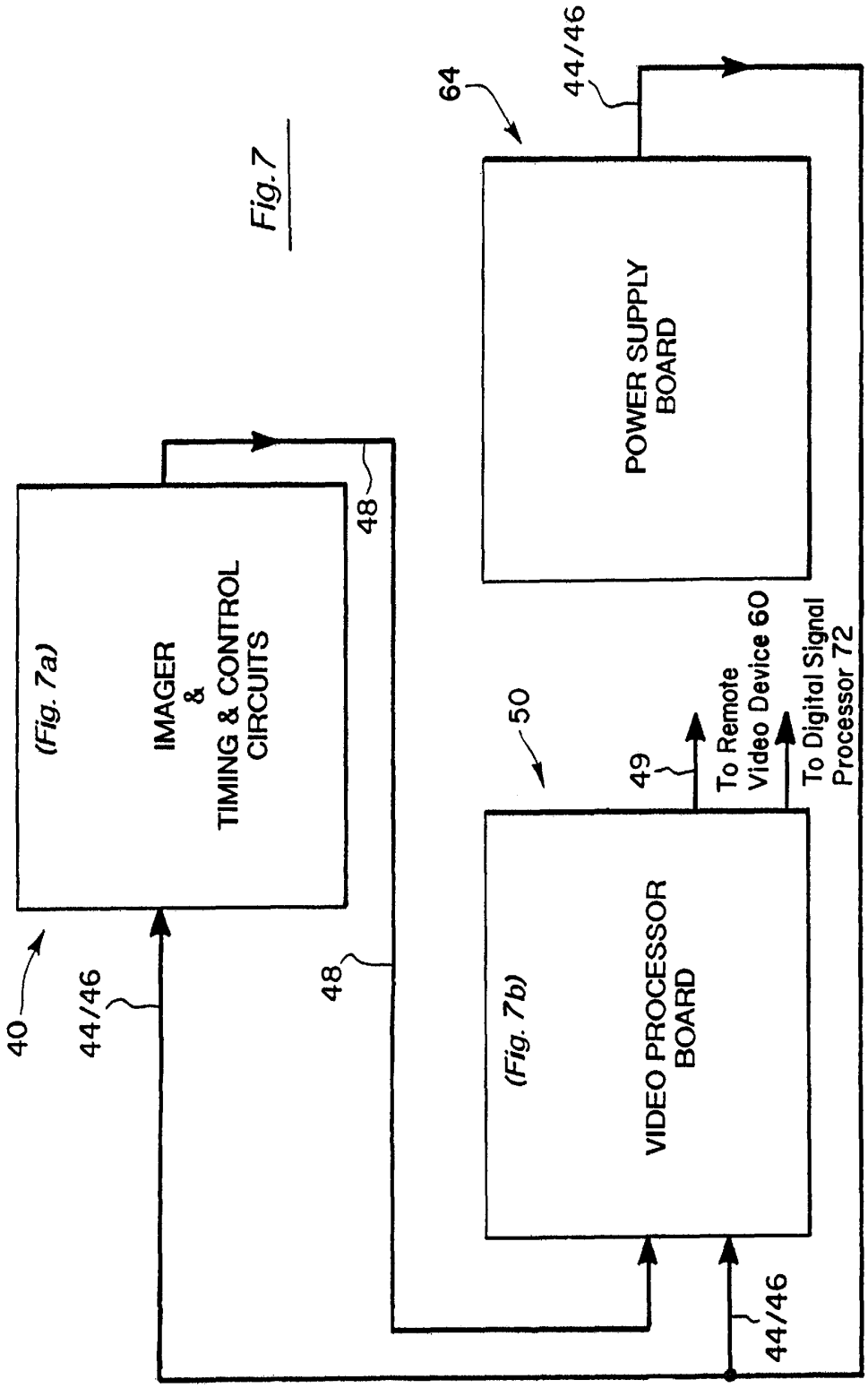


Fig_6b

Fig. 7


64
44/46
POWER SUPPLY BOARD
48
(Fig. 7a)
IMAGER & TIMING & CONTROL CIRCUITS
50
49
To Remote Video Device 60
To Digital Signal Processor 72
40
44/46
48
(Fig. 7b)
VIDEO PROCESSOR BOARD
44/46

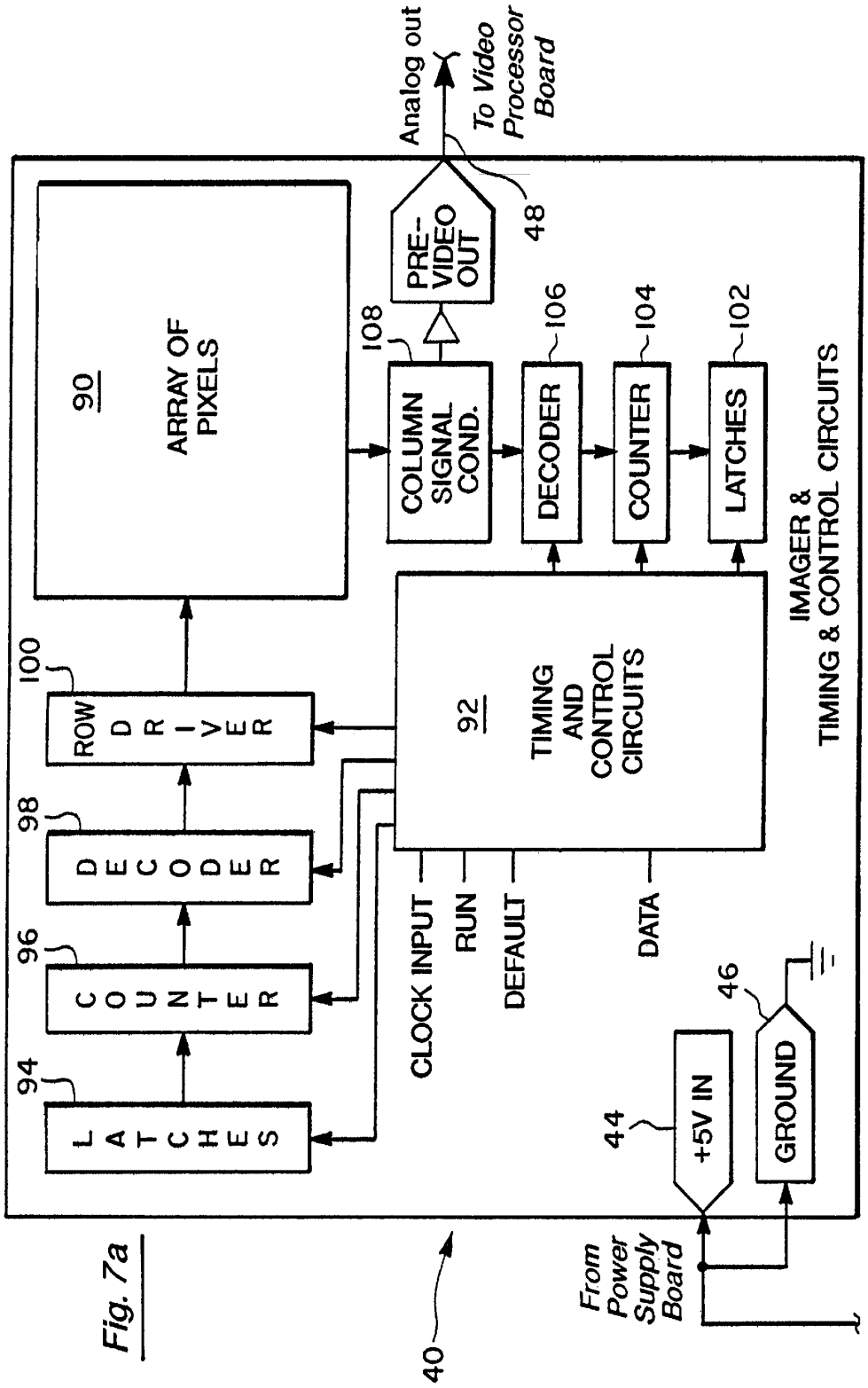
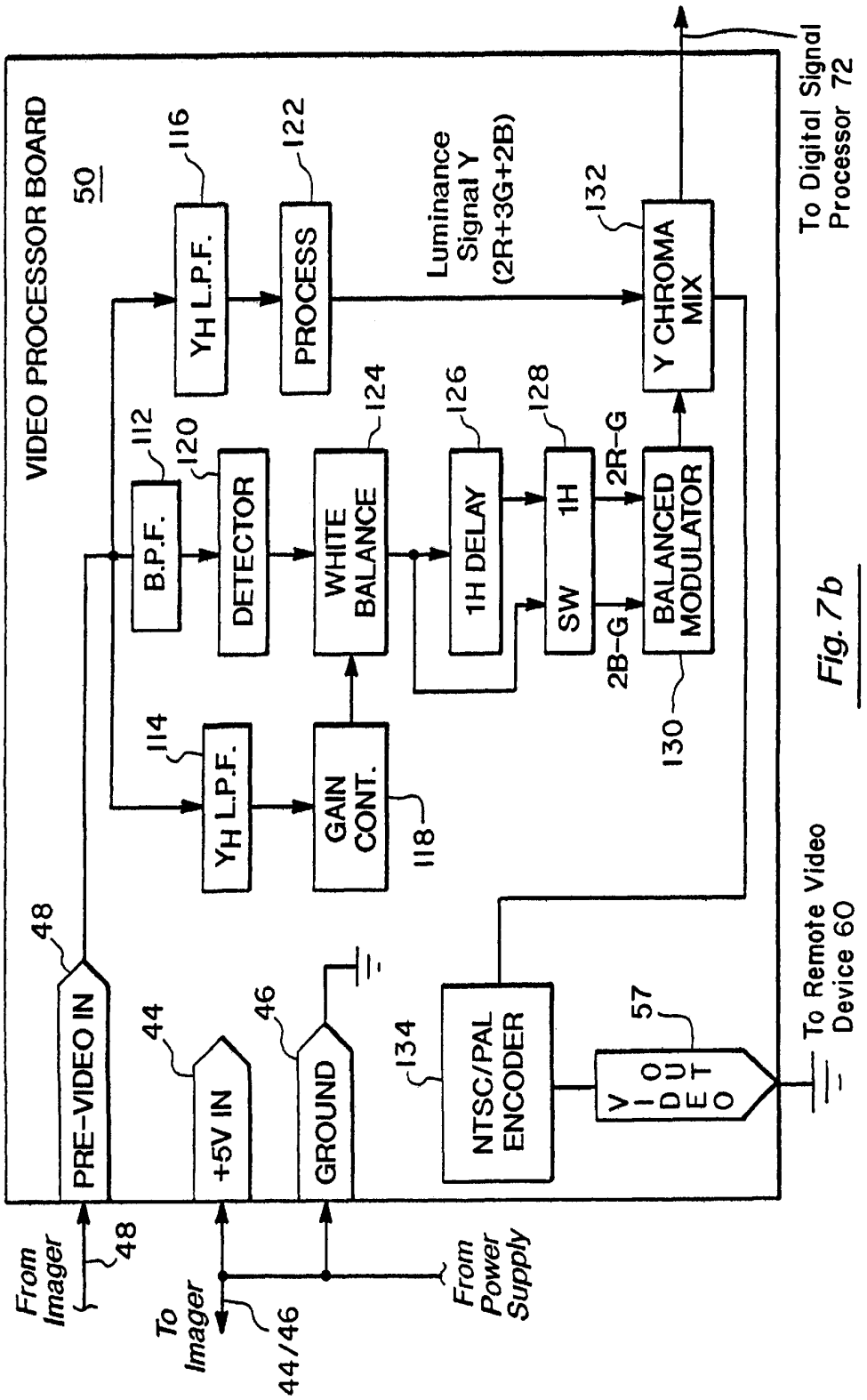

Analog out
To Video Processor Board
48
PRE-VIDEO OUT
108
106
104
102
90
ARRAY OF PIXELS
COLUMN SIGNAL COND.
DECODER
COUNTER
LATCHES
IMAGER & TIMING & CONTROL CIRCUITS
100
ROW DRIVER
92
TIMING AND CONTROL CIRCUITS
98
DECODER
96
COUNTER
94
LATCHES
CLOCK INPUT
RUN
DEFAULT
DATA
46
44
+5V IN
GROUND
From Power Supply Board
40

Fig. 7a


VIDEO PROCESSOR BOARD
50
PRE-VIDEO IN
48
+5V IN
44
GROUND
46
B.P.F.
112
DETECTOR
120
YH L.P.F.
116
PROCESS
122
YH L.P.F.
114
GAIN CONT.
118
WHITE BALANCE
124
1H DELAY
126
SW 1H
128
2R-G
2B-G
BALANCED MODULATOR
130
Y CHROMA MIX
132
Luminance Signal Y (2R+3G+2B)
NTSC/PAL ENCODER
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VIDEO OUT
57
To Digital Signal Processor 72
To Remote Video Device 60
From Imager
48
To Imager
44/46
From Power Supply

Fig. 7b

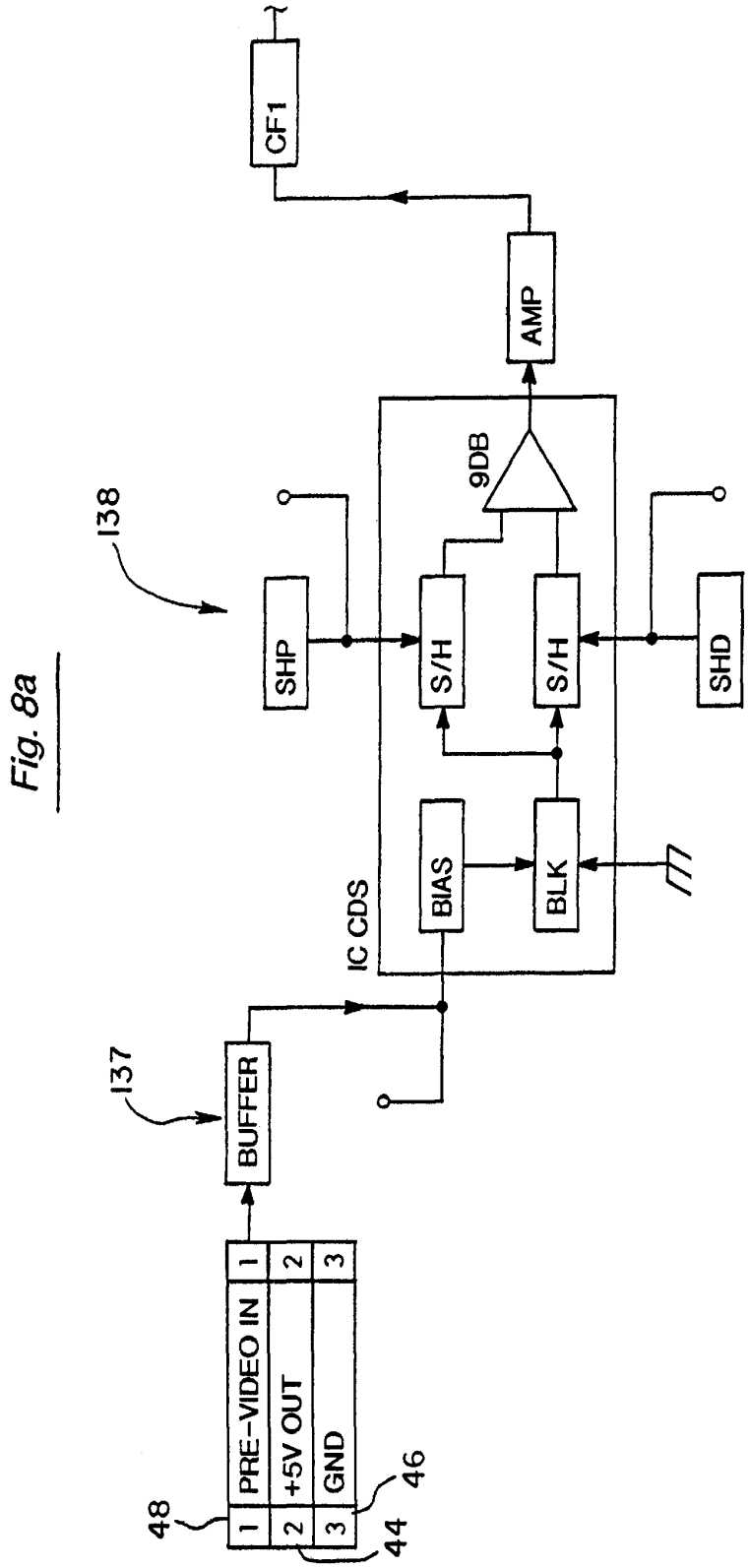

CF1
AMP
9DB
138
SHP
S/H
S/H
SHD
BIAS
BLK
IC CDS
137
BUFFER
1
2
3
PRE-VIDEO IN
+5V OUT
GND
48
46
44

Fig. 8a

Fig. 8b

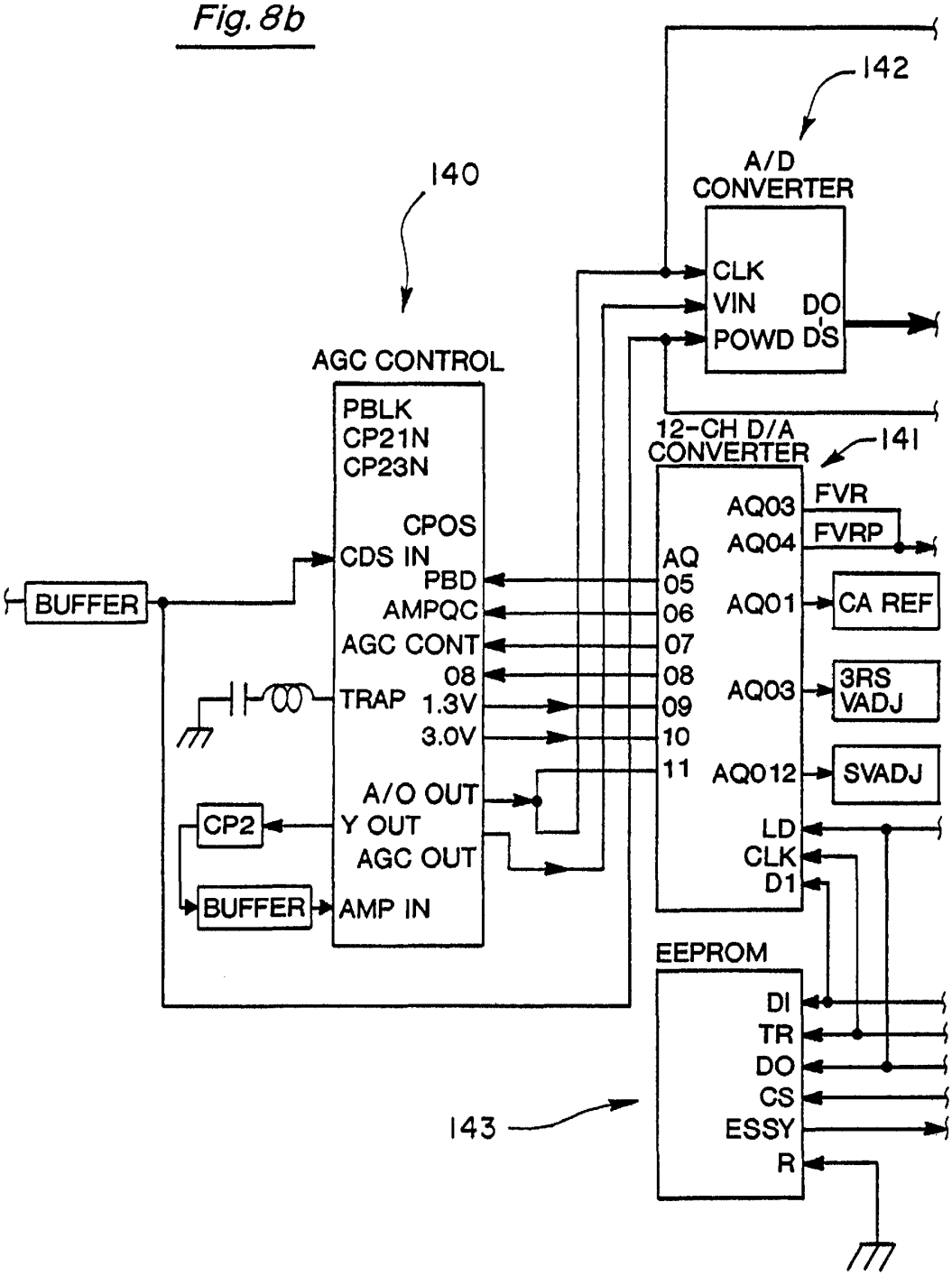
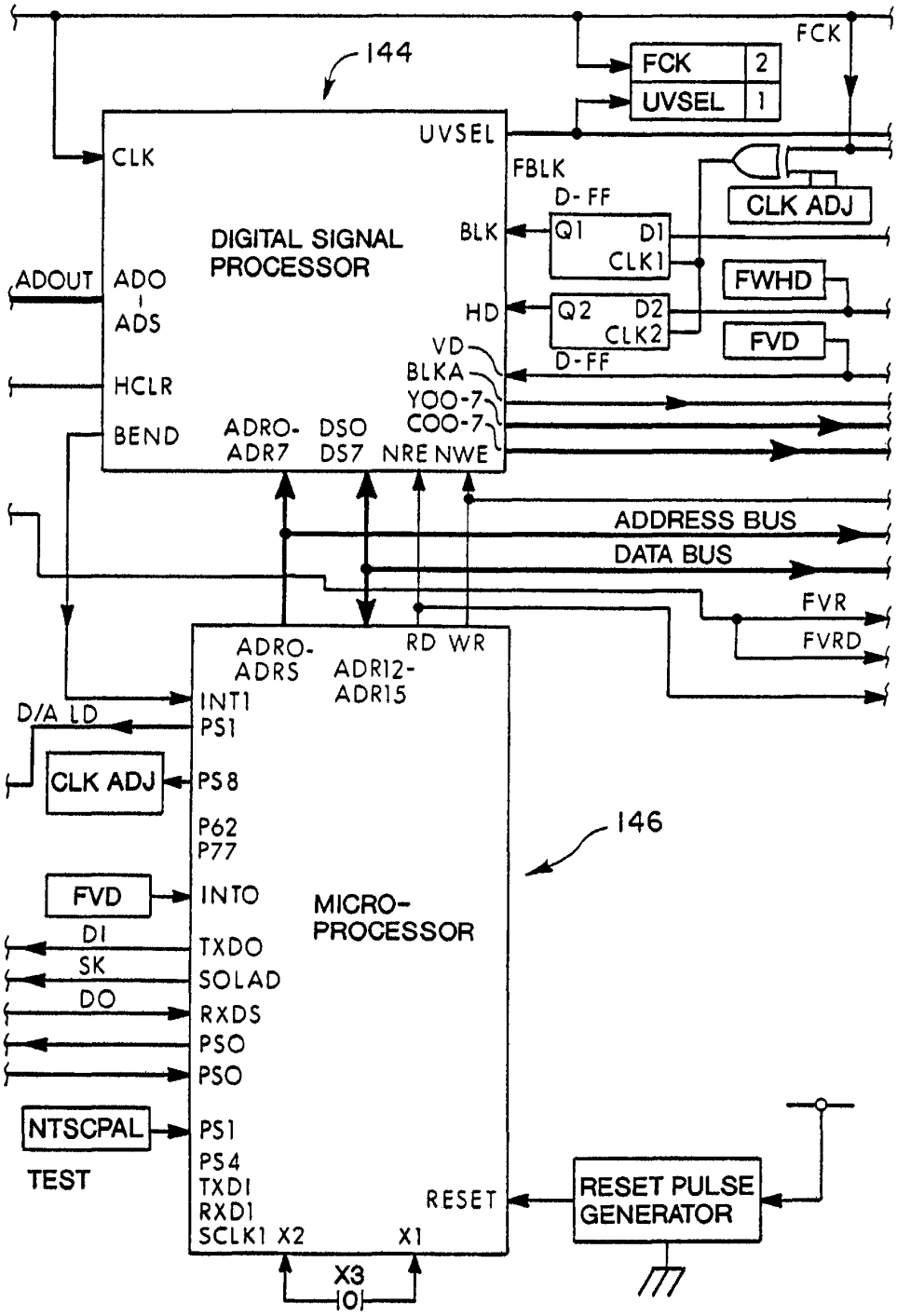

142
A/D CONVERTER
CLK
VIN
POWD
DO
DS
140
AGC CONTROL
PBLK
CP21N
CP23N
CPOS
CDS IN
PBD
AMPQC
AGC CONT
TRAP
08
1.3V
3.0V
A/O OUT
Y OUT
AGC OUT
AMP IN
BUFFER
CP2
BUFFER
12-CH D/A CONVERTER
141
AQ 05
06
07
08
09
10
11
AQ03
AQ04
AQ01
AQ03
AQ012
FVR
FVRP
CA REF
3RS VADJ
SVADJ
LD
CLK
D1
EEPROM
DI
TR
DO
CS
ESSY
R
143

Fig. 8c


144
FCK
FCK 2
UVSEL 1
UVSEL
CLK
FBLK
D-FF
CLK ADJ
DIGITAL SIGNAL PROCESSOR
BLK
Q1 D1 CLK1
FWHD
ADOUT
ADO
ADS
HD
Q2 D2 CLK2
FVD
VD
D-FF
BLKA
HCLR
YOO-7
BEND
ADRO-ADR7
DSO DS7
COO-7
NRE NWE
ADDRESS BUS
DATA BUS
FVR
FVRD
RD WR
ADRO-ADRS
ADR12-ADR15
INT1
D/A LD
PS1
CLK ADJ
PS8
P62
P77
146
FVD
INTO
MICRO-PROCESSOR
DI
TXDO
SK
SOLAD
DO
RXDS
PSO
PSO
NTSCPAL
PS1
TEST
PS4
TXDI
RXDI
RESET
RESET PULSE GENERATOR
SCLK1 X2
X1
X3

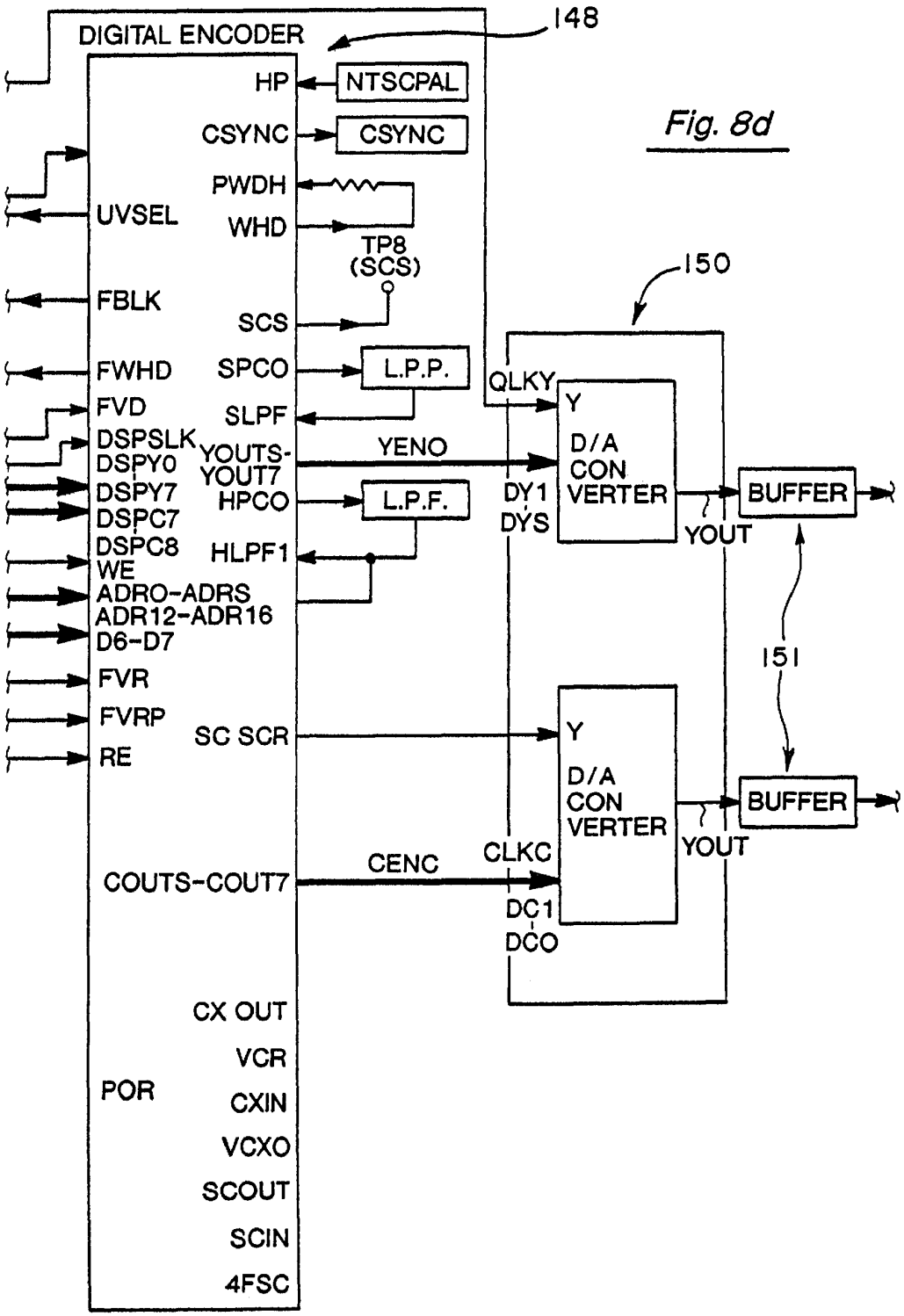

DIGITAL ENCODER
148
HP
NTSCPAL
CSYNC
CSYNC
PWDH
UVSEL
WHD
TP8
(SCS)
FBLK
SCS
150
FWHD
SPCO
L.P.P.
QLKY
FVD
SLPF
Y
DSPSLK
YOUTS-
YENO
D/A
DSPY0
YOUT7
CON
DSPY7
HPCO
L.P.F.
DY1
VERTER
BUFFER
DSPC7
DYS
YOUT
DSPC8
HLPF1
WE
ADRO-ADRS
ADR12-ADR16
D6-D7
151
FVR
FVRP
SC SCR
Y
RE
D/A
CON
VERTER
BUFFER
CLKC
YOUT
CENC
COUTS-COUT7
DC1
DCO
CX OUT
VCR
POR
CXIN
VCXO
SCOUT
SCIN
4FSC

Fig. 8d

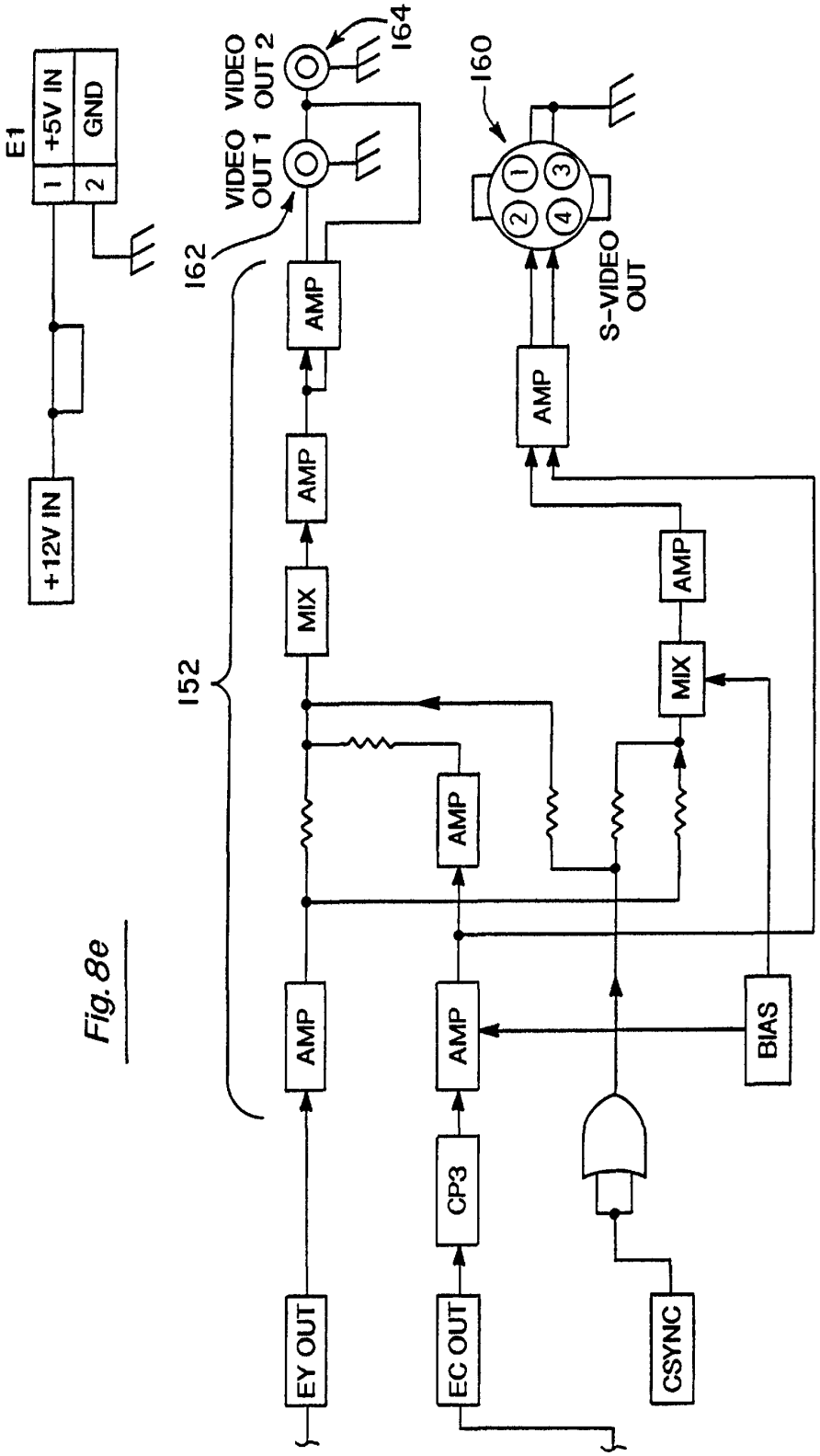

E1
+5V IN
GND
1
2
+12V IN
VIDEO OUT 2
VIDEO OUT 1
164
162
160
S-VIDEO OUT
1
2
3
4
AMP
MIX
152
BIAS
CP3
EY OUT
EC OUT
CSYNC

Fig. 8e

HAND-HELD COMPUTERS INCORPORATING REDUCED AREA IMAGING DEVICES

This application is a continuation-in-part of U.S. Ser. No. 09/496,312, filed Feb. 1, 2000, and entitled "Reduced Area Imaging Devices", which is a continuation application of U.S. Ser. No. 09/175,685, filed Oct. 20, 1998 and entitled "Reduced Area Imaging Devices", now U.S. Pat. No. 6,043,839, which is a continuation-in-part of U.S. Ser. No. 08/944,322, filed Oct. 6, 1997 and entitled "Reduced Area Imaging Devices Incorporated Within Surgical Instruments", now U.S. Pat. No. 5,929,901.

TECHNICAL FIELD

This invention relates to solid state image sensors and associated electronics, and more particularly, to solid state image sensors which are configured to be of a minimum size and used within miniature computer systems known as palm top computers, personal digital assistants (PDA), or hand-held computers/organizers.

BACKGROUND ART

The three most common solid state image sensors include charged coupled devices (CCD), charge injection devices (CID) and photo diode arrays. In the mid-1980s, complementary metal oxide semiconductors (CMOS) were developed for industrial use. CMOS imaging devices offer improved functionality and simplified system interfacing. Furthermore, many CMOS imagers can be manufactured at a fraction of the cost of other solid state imaging technologies.

The CCD device is still the preferred type of imager used in scientific applications. Only recently have CMOS-type devices been improved such that the quality of imaging compares to that of CCD devices. However, there are enormous drawbacks with CCD devices. Two major drawbacks are that CCD device have immense power requirements, and the amount of processing circuitry required for a CCD imager always requires the use of a remote processing circuitry module which can process the image signal produced by the CCD imager. Also, because of the type of chip architecture used with CCD devices, on-chip processing is impossible. Therefore, even timing and control circuitry must be remoted from the CCD imager plane. Therefore, CCD technology is the antithesis of "camera on a chip" technology discussed below.

One particular advance in CMOS technology has been in the active pixel-type CMOS imagers which consist of randomly accessible pixels with an amplifier at each pixel site. One advantage of active pixel-type imagers is that the amplifier placement results in lower noise levels. Another major advantage is that these CMOS imagers can be mass produced on standard semiconductor production lines. One particularly notable advance in the area of CMOS imagers including active pixel-type arrays is the CMOS imager described in U.S. Pat. No. 5,471,515 to Fossum, et al. This CMOS imager can incorporate a number of other different electronic controls that are usually found on multiple circuit boards of much larger size. For example, timing circuits, and special functions such as zoom and anti-jitter controls can be placed on the same circuit board containing the CMOS pixel array without significantly increasing the overall size of the host circuit board. Furthermore, this particular CMOS imager requires 100 times less power than a CCD-type imager. In short, the CMOS imager disclosed in Fossum, et al. has enabled the development of a "camera on a chip."

Passive pixel-type CMOS imagers have also been improved so that they too can be used in an imaging device which qualifies as a "camera on a chip." In short, the major difference between passive and active CMOS pixel arrays is that a passive pixel-type imager does not perform signal amplification at each pixel site. One example of a manufacturer which has developed a passive pixel array with performance nearly equal to known active pixel devices and compatible with the read out circuitry disclosed in the U.S. Pat. No. 5,471,515 is VLSI Vision, Ltd., 1190 Saratoga Avenue, Suite 180, San Jose, Calif. 95129. A further description of this passive pixel device may be found in co-pending application, Ser. No. 08/976,976, entitled "Reduced Area Imaging Devices Incorporated Within Surgical Instruments," now U.S. Pat. No. 5,986,693, and is hereby incorporated by reference.

In addition to the active pixel-type CMOS imager which is disclosed in U.S. Pat. No. 5,471,515, there have been developments in the industry for other solid state imagers which have resulted in the ability to have a "camera on a chip." For example, Suni Microsystems, Inc. of Mountain View, Calif., has developed a CCD/CMOS hybrid which combines the high quality image processing of CCDs with standard CMOS circuitry construction. In short, Suni Microsystems, Inc. has modified the standard CMOS and CCD manufacturing processes to create a hybrid process providing CCD components with their own substrate which is separate from the P well and N well substrates used by the CMOS components. Accordingly, the CCD and CMOS components of the hybrid may reside on different regions of the same chip or wafer. Additionally, this hybrid is able to run on a low power source (5 volts) which is normally not possible on standard CCD imagers which require 10 to 30 volt power supplies. A brief explanation of this CCD/CMOS hybrid can be found in the article entitled "Startup Suni Bets on Integrated Process" found in *Electronic News,* Jan. 20, 1997 issue. This reference is hereby incorporated by reference for purposes of explaining this particular type of imaging processor.

Another example of a recent development in solid state imaging is the development of a CMOS imaging sensor which is able to achieve analog to digital conversion on each of the pixels within the pixel array. This type of improved CMOS imager includes transistors at every pixel to provide digital instead of analog output that enable the delivery of decoders and sense amplifiers much like standard memory chips. With this new technology, it may, therefore, be possible to manufacture a true digital "camera on a chip." This CMOS imager has been developed by a Stanford University joint project and is headed by Professor Abbas el-Gamal.

A second approach to creating a CMOS-based digital imaging device includes the use of an over-sample converter at each pixel with a one bit comparator placed at the edge of the pixel array instead of performing all of the analog to digital functions on the pixel. This new design technology has been called MOSAD (multiplexed over sample analog to digital) conversion. The result of this new process is low power usage, along with the capability to achieve enhanced dynamic range, possibly up to 20 bits. This process has been developed by Amain Electronics of Simi Valley, Calif. A brief description of both of the processes developed by Stanford University and Amain Electronics can be found in an article entitled "A/D Conversion Revolution for CMOS Sensor?," September 1998 issue of *Advanced Imaging.* This article is also hereby incorporated by reference for purposes of explaining these particular types of imaging processors.

Yet another example of a recent development with respect to solid state imaging is an imaging device developed by ShellCase, of Jerusalem, Israel. In an article entitled "A CSP Optoelectronic Package for Imaging and Light Detection Applications" (A. Badihi), ShellCase introduces a diesized, ultrathin optoelectronic package which is completely packaged at the wafer level using semiconductor processing. In short, ShellCase provides a chip scale package (CSP) process for accepting digital image sensors which may be used, for example, in miniature cameras. The die-sized, ultrathin package is produced through a wafer level process which utilizes optically clear materials and completely encases the imager die. This packaging method, ideally suited for optoelectronic devices, results in superior optical performance and form factor not available by traditional image sensors. This article is also incorporated by reference for purposes of explaining ShellCase's chip scale package process.

Yet another example of a recent development with respect to solid state imaging is shown in U.S. Pat. No. 6,020,581 entitled "Solid State CMOS Imager Using Silicon on Insulator or Bulk Silicon." This patent discloses an image sensor incorporating a plurality of detector cells arranged in an array wherein each detector cell as a MOSFET with a floating body and operable as a lateral bipolar transistor to amplify charge collected by the floating body. This invention overcomes problems of insufficient charge being collected in detector cells formed on silicon on insulator (SOI) substrates due to silicon thickness and will also work in bulk silicon embodiments.

The above-mentioned developments in solid state imaging technology have shown that "camera on a chip" devices will continue to be enhanced not only in terms of the quality of imaging which may be achieved, but also in the specific construction of the devices which may be manufactured by new breakthrough processes.

Although the "camera on a chip" concept is one which has great merit for application in many industrial areas, a need still exists for a reduced area imaging device which can be used in even the smallest type of industrial application. Recently, devices known as palm top computers, PDA(s), or hand-held computers have become very popular items. Essentially, these PDAs are miniature computers, small enough to be held in the hand, which have various software programs available to a user including word processing, e-mail, and organization software for addresses/phone books, etc.

One example of a U.S. patent disclosing a type of a PDA includes U.S. Pat. No. 5,900,875. This patent is incorporated herein by reference for purposes of illustrating an example of a PDA including basic functionality for such a device. In a recent article entitled "Palm, Inc. Gets Ready for New Hands" appearing in the *Wallstreet Journal,* a number of soon to be commercially available PDAs are disclosed. One such device disclosed in this article is known as the "Hand Spring Visor Deluxe." This device will soon be available which allows a user to accommodate pagers, MP3 players, still digital cameras and other devices.

It is one general object of this invention to provide a video system in combination with a standard PDA enabling a user to take video images by a very small camera module incorporated within the PDA, view the video images taken on a video viewscreen incorporated within the PDA, and to have the capability to store, download the video images, and send the video images electronically through a communications network.

Another object of this invention is to provide a PDA with the ability to not only transmit video images taken by the camera module, but also to receive video images sent from a remote location via the communications network, and to view such received video images on the video view screen of the PDA. Accordingly, the invention is ideally suited for video teleconferencing.

It is another object of this invention to provide a reduced area imaging device incorporated within a PDA which takes advantage of "camera on a chip" technology, but to rearrange the video processing circuitry in a selective stacked relationship so that the camera module has a minimum profile.

It is yet another object of this invention to provide imaging capability for a PDA wherein the video camera used is of such small size that it can be stored in the PDA when not in use. The camera module is attached to the PDA by a retractable cord which enables the imaging device to be used to image anything at which the camera module is pointed by the user without having to also move the PDA away from the view of the user.

In all applications, to include use of the imaging device of this invention with a PDA, "camera on a chip" technology can be improved with respect to reducing its profile area, and incorporating such a reduced area imaging device within a PDA such that minimal size and weight is added to the PDA, and further that the imaging device can be used to image selected targets by the user.

DISCLOSURE OF THE INVENTION

In accordance with the present invention, reduced area imaging devices are provided in combination with a hand-held computer or PDA. The term "imaging device" as used herein describes the imaging elements and processing circuitry which is used to produce a video signal which may be accepted by both a standard video device such as a television or video monitor accompanying a personal computer, and a small LCD screen which is incorporated within the PDA. The term "image sensor" as used herein describes the components of a solid state imaging device which captures images and stores them within the structure of each of the pixels in the array of pixels found in the imaging device. As further discussed below, the timing and control circuits can be placed either on the same planar structure as the pixel array, in which case the image sensor can also be defined as an integrated circuit, or the timing and control circuitry can be placed remote from the pixel array. The terms "video signal" or "image signal" as used herein, and unless otherwise more specifically defined, refer to an image which at some point during its processing by the imaging device, is found in the form of electrons which have been placed in a specific format or domain. The term "processing circuitry" as used herein refers to the electronic components within the imaging device which receive the image signal from the image sensor and ultimately place the image signal in a usable format. The terms "timing and control circuits" or "timing and control circuitry" as used herein refer to the electronic components which control the release of the image signal from the pixel array.

In a first arrangement, the image sensor, with or without the timing and control circuitry, may be placed at the distal tip of a very small camera module which is attached by a cable or cord to the PDA, while the remaining processing circuitry may be placed within the housing of the PDA.

In a second arrangement, the image sensor and the processing circuitry may all be placed in a stacked arrangement of miniature circuit boards or planar circuit structures and positioned at the distal tip of the camera module. In this

second arrangement, the pixel array of the image sensor may be placed by itself on its own circuit board while the timing and control circuitry and processing circuitry are placed on one or more other circuit boards, or the circuitry for timing and control may be placed with the pixel array on one circuit board, while the remaining processing circuitry can be placed on one or more of the other circuit boards.

In yet another alternative arrangement, the pixel array, timing and control circuits, and some of the processing circuitry can be placed near the distal end of the camera module on two or more circuit boards with the remaining part of the processing circuitry being placed in the housing of the PDA.

For the arrangement or configuration of the imaging device which calls for the array of pixels and the timing and control circuitry to be placed on the same circuit board, only one conductor is required in order to transmit the image signal to the video processing circuitry. When the timing and control circuits are incorporated onto other circuit boards, a plurality of connections are required in order to connect the timing and control circuitry to the pixel array, and then the one conductor is also required to transmit the image signal back to the video processing circuitry.

As mentioned above, the invention disclosed herein can be considered an improvement to a PDA wherein the improvement comprises a video system. The video system would include the video view screen or monitor attached to the PDA, the camera module, as well as supporting video processing circuitry for the imaging device. In yet another aspect, the invention disclosed herein can also be considered an improvement to a PDA wherein the improvement comprises a novel imaging device, preferably of CMOS construction. For this improvement comprising the imaging device, the imaging device includes the array of pixels, and the supporting video processing circuitry for providing a video ready signal.

This video ready signal may be formatted by the video processing circuitry for viewing on a NTSC/PAL compatible device such as television, or for viewing on a VGA compatible device such as a monitor of a personal computer. Of course, the video ready signal is formatted for viewing the video images on the video view screen incorporated within the PDA.

In yet another aspect, the invention disclosed herein can also be considered an improvement to a PDA wherein the improvement comprises a combination of a video system, and wireless telephone communication means for transmitting and receiving both audio and video signals. In this aspect, the invention has functionality for transmitting and receiving audio and video signals via the communications network. One example of a U.S. patent disclosing wireless remote communications between a personal computer and a PDA or miniature hand held computer is U.S. Pat. No. 6,034,621. This patent is hereby incorporated by reference in its entirety for purposes of disclosing means by which data can be exchanged between the hand held computer and a personal computer, to include video and audio signals. The specific example in this patent which readily lends itself to the communication network incorporated within this invention is found at FIG. 4 of this '621 patent. The discussion further below outlines this particular communication network.

In yet another aspect, the invention disclosed herein can also be considered an improvement to a PDA wherein the improvement comprises a video system, and a standard wireless telephone communication means for transmitting and receiving audio signals. In this aspect, the PDA simply includes a standard wireless/cellular phone connected externally on the PDA which enables the user to conduct well-known wireless/telephone communications. This wireless/cellular communication means can be in addition to the wireless telephone communication means for transmitting and receiving both audio and video signals discussed immediately above with respect to the U.S. Pat. No. 6,034,621.

Another example of a U.S. patent disclosing basic mobile phone technology including a discussion of basic phone circuitry is U.S. Pat. No. 6,018,670. This patent is hereby incorporated by reference in its entirety for purposes of disclosing standard or basic mobile phone technology and supporting circuitry.

Accordingly, the invention disclosed herein has utility with respect to an overall combination of elements, as well as various sub-combination of elements.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an enlarged fragmentary partially exploded perspective view of the distal end of the camera module which is used in conjunction with the PDA, specifically illustrating the arrangement of the image sensor with respect to the other elements of the camera module;

FIG. **1***a* is an enlarged exploded perspective view illustrating another configuration of the image sensor wherein video processing circuitry is placed behind and in longitudinal alignment with the image sensor;

FIG. **2** is a perspective view of the PDA incorporating the reduced area imaging device of this invention;

FIG. **3** illustrates the PDA of FIG. **2** wherein the camera module is in the retracted position;

FIG. **4** is an overall schematic diagram of the functional electronic components which make up both the PDA and the reduced area imaging device wherein communications are achieved by wireless/cellular technology for video teleconferencing via the world wide web which is well-known as a global communications network;

FIG. **5** is a schematic diagram illustrating an example communications network which can be used for data transfer of text, audio, and visual signals between the PDA and a personal computer which is in communication with the world wide web;

FIG. **6***a* is a perspective view of the PDA in combination with an externally attached wireless/cellular phone;

FIG. **6***b* is another perspective view of the combination of FIG. **6***a* illustrating the combination opened to expose the PDA;

FIG. **7** is a more detailed schematic diagram of the functional electronic components which make up the imaging device;

FIG. **7***a* is an enlarged schematic diagram of a circuit board/planar structure which may include the array of pixels and the timing and control circuitry;

FIG. **7***b* is an enlarged schematic diagram of a video processing board/planar structure having placed thereon the processing circuitry which processes the pre-video signal generated by the array of pixels and which converts the pre-video signal to a post-video signal which may be accepted by an NTSC/PAL compatible video device; and

FIGS. **8***a*–**8***e* are schematic diagrams that illustrate an example of specific circuitry which may be used to make the video processing circuitry of the imaging device.

BEST MODE FOR CARRYING OUT THE INVENTION

In accordance with the invention, as shown in FIG. **1**, a camera module **10** is provided which incorporates a reduced

area imaging device **11**. As further discussed below, the elements of the imaging device **11** may all be found near one location, or the elements may be separated from one another and interconnected by the appropriate wired connections. The array of pixels making up the image sensor captures images and stores them in the form of electrical energy by conversion of light photons to electrons. This conversion takes place by the photo diodes in each pixel which communicate with one or more capacitors which store the electrons. Specifically, the camera module **10** includes an outer tube/sheath **14** which houses the components of the imaging device. The camera module is shown as being cylindrical in shape having a window **16** sealed at the distal end of the camera module. A retractable cable **12** extends from the proximal end of the camera module **10**. A shielded cable **21** is used to house the conductors which communicate with the imaging device **11**. The shielded cable **21** is then housed within the retractable cable **12**. A lens group **18** is positioned at the distal end of the camera module to enable an image to be appropriately conditioned prior to the image impinging upon the imaging device **11**. Also shown is a focusing ring **20** which enables the lens group **18** to be displaced distally or proximally to best focus an image on the imaging device **11**.

Now referring to FIGS. **2** and **3**, a PDA **22** is shown which incorporates the camera module **10**. In basic terms, the PDA **22** is a miniature hand-held computer incorporating a video system enabling video to be taken by the camera module, and viewed on the video view screen **26**, as well as enabling images to be stored and downloaded on a miniature computer disc (not shown) used with the PDA. Also discussed further below is the ability to transmit and receive audio and video signals.

Beginning first with a description of the basic components of the PDA **22**, it includes a housing **24** which hold the components of the PDA and the video system. Cable **12** is housed within the housing **24** when in the retracted position. A spring biased spool (not shown) or some other known retracting device is mounted within the housing **24** enabling the cable **12** to be extended or retracted. A plurality of controls are provided enabling the user to manipulate the functions of the PDA. These are shown as buttons **34** on the housing **24**. The video view screen **26** is used for displaying video images taken by the camera module **10**, or for viewing incoming video signals received from a remote location. A command screen **28** is provided which allows a user to select programs with a stylus (not shown). A video capture button **30** is provided which allows a user to capture a still video image taken by the camera module **10**. A video store button **32** is also provided which enables a captured video image to be stored within the digital memory of the PDA, as further discussed below. An opening or cavity **35** is provided which allows the camera module **10** to be stored, along with cable **12** within the housing **24**. As shown in FIG. **3**, the camera module **10** is in the stored or retracted position. The antenna **36** allows for enhanced transmission and reception of incoming or transmitted/outgoing audio and video signals. A video select switch **37** is provided enabling a user to view either video images taken by the camera module **10**, or for viewing incoming video images. The video view screen **26** may be a liquid crystal display (LCD) type, or any other well-known display device of high resolution which has low power requirements, and has minimum size requirements as well.

An example of a manufacture of such a miniature LCD monitor includes DISPLAYTECH of Longmont, Colo. DISPLAYTECH manufactures a miniature reflective display that consists of ferroelectric liquid crystal (FLC) applied to a CMOS integrated circuit. The reflective display is a VGA display panel having low voltage digital operation, low power requirements, and full color operation. One of their specific products includes the LightCaster™ VGA Display Panel, Model LDP-0307-MV1. This is but one example of an LCD monitor which is available and usable within the invention herein described.

A camera on/off switch **66** is provided enabling the user to turn the video system on or off. Also shown in FIGS. **2** and **3** is a speaker **76** and a microphone **78** which are used for sending and receiving audio signals in the conventional manner as with a wireless/cellular telephone. A further description of speaker **76** and microphone **78** is found below.

Referring back to FIGS. **1** and **1***a*, the imaging device **11** includes an image sensor **40**. FIG. **1** illustrates that the image sensor **40** can be a planar and square shaped member, or alternatively, planar and circular shaped to better fit within outer tube **14**. In the configuration of the imaging device in FIGS. **1** and **1***a*, there are only three conductors which are necessary for providing power to the image sensor **40**, and for transmitting an image from the image sensor **40** back to the processing circuitry found within the phone housing **24**. Specifically, there is a power conductor **44**, a grounding conductor **46**, and an image signal conductor **48**, each of which are hardwired to the image sensor **40**. Thus, shielded cable **21** may simply be a three conductor, 50 ohm type cable.

Image sensor **40** can be as small as 1 mm in its largest dimension. However, a more preferable size for most PDA applications would be between 4 mm to 8 mm in the image sensor's largest dimension (height or width). The image signal transmitted from the image sensor **40** through conductor **48** is also herein referred to as a pre-video signal. Once the pre-video signal has been transmitted from image sensor **40** by means of conductor **48**, it is received by video processing board **50**, as shown in FIG. **7**. Video processing board **50** then carries out all the necessary conditioning of the pre-video signal and places it in a form, also referred to herein as a video ready signal, so that it may be viewed directly on a remote video device such as a television or standard computer video monitor. In order for the pre-video signal to be viewed on the video view screen/monitor **26**, the pre-video signal is further conditioned by a digital signal processor **72**, as further discussed below. The video signal produced by the video processing board **50** can be viewed by an NTSC/PAL compatible video device (such as a television) which connects to the PDA through a remote jack. This video signal produced by board **50** can be further defined as a post-video signal.

FIG. **1** illustrates an arrangement wherein the image sensor **40** is placed by itself adjacent the distal end of the camera module **10**. Alternatively, some or all of the video processing circuitry may be placed in adjacent circuit boards directly behind the image sensor **40**. Accordingly, **1***a* illustrates video processor board **50** aligned directly behind the image sensor **40**. A plurality of pin connectors **52** can be used to interconnect image sensor **40** to video processor board **50**. Depending upon the specific configuration of image sensor **40**, pin connectors **52** may be provided for structural support only, and/or to provide a means by which image signals are transmitted between image sensor **40** and board **50**. Additionally, digital signal processor **72** could also be placed behind image sensor **40** and behind video processing board **50**. Accordingly, the image sensor, and all supporting video processing circuitry could be placed at the distal end of the camera module **10**. However, because of the

ample space within housing **24**, it may be preferable to place at least some of the video processing circuitry within housing **24**. In the case of FIG. **1***a,* the conductor **49** represents the conductor which may carry the post-video signal for direct connection with a remote video device **60** such as a television or computer monitor. As also discussed further below, placement of the digital signal processor **72** at the distal tip of the camera module behind the video processing board **50** would also enable yet another conductor (not shown) to connect directly to the video monitor **26** for transmitting a video signal to the video monitor **26**.

Again referring to FIGS. **1** and **1***a,* the area which is occupied by image sensor **40** may be defined as the profile area of the imaging device and which determines its critical dimensions. If it is desired to place video processing circuitry adjacent the image sensor **40** at the distal end of the camera module **10**, such circuitry must be able to be placed on one or more circuit boards which are longitudinally aligned with image sensor **40** along longitudinal axis XX. If it is not important to limit the size of the profile area, then any circuitry placed behind image sensor **40** can be aligned in an offset manner, or may simply be larger than the profile area of image sensor **40**. In the configuration shown in FIG. **1***a,* it is desirable that elements **40** and **50** be approximately the same size so that they may uniformly fit within the distal end of outer tube **14**.

Now referring to FIG. **4**, a further explanation is provided of the basic electronic components of the PDA **22**. The PDA **22** of this invention includes functionality normally found in multiple devices. Specifically, the PDA **22** includes the computing capability of a PDA, a mobile/wireless phone, communication means for connection to a computer network such as the worldwide web, and a video system. The PDA **22** may be separated into two major groups, namely, a video and communication system **61**, and a computer processing and memory unit **82**. Both of these are discussed in further detail below.

As shown in FIG. **4**, a conventional lithium ion battery **62** is provided which communicates with power supply board **64**. Power supply board **64** conditions various power outputs to the components of the device, to include power to the video components. In the preferred imaging device of this invention, the power to the imaging device may simply be direct current of between about 1.5 to 12 volts, depending upon the power requirements of the imaging device. A camera on/off switch **66** must be set to the "on" position in order to activate the camera module **10**. The video processor board **50** then transfers power to supplies the camera module **10**, and also receives the analog pre-video signal back from the camera module, as further discussed below. After processing of the pre-video signal at the video processor board **50**, the video signal is video ready, meaning that it may then be directly viewed on a remote compatible video device **60**, such as a television or computer monitor. A video port **54** can be provided on the housing **24** enabling a user to take a standard video jack (not shown) and interconnect the PDA with the video port of the remote video device. The video format for such remote video devices includes NTSC/PAL and VGA; thus, the video signal processed by video processor board **50** creates the video ready signals for use with these remote video devices. For purposes of viewing images on the monitor **26**, the pre-video signal is further processed into a digital format within video processor board **50**, preferably an 8 bit component video signal format that is commonly referred to as "YUV 4:2:2." This video format easily lends itself to video compression. This 8 bit digital video signal is then sent to the digital signal processor **72** which performs two functions relevant to the video signal. The digital signal processor **72** further converts the signal into a format that is compatible with the driver circuitry of the video monitor **26**. Secondly, the digital signal processor **72** compresses the YV signal using a common video compression format, preferably JPEG. The JPEG encoded video signal is then mixed with the audio signal created by microphone **78** and amplifier **74**, and the resulting high frequency carrier signal may then be passed onto the transceiver/amplifier section **70** for transmission. It is to be understood that the transceiver/amplifier **70** is intended for communication with well-known wide area wireless communication networks. It is also contemplated within the spirit and scope of this invention that the PDA **22** be capable of communication with computer networks to include the worldwide web. Accordingly, the invention is well adapted for conducting video teleconferencing which is normally conducted with desktop computers and supplemental video equipment. The transceiver/amplifier section also modulates the carrier signal prior to transmission. Depending upon the position of video switch **37**, the video signal from digital signal processor **72** is either sent to the monitor **26**, or is sent to the transceiver/amplifier section **70** for transmission. As also shown, the antenna **36** is used for enhancement of reception and transmission of transmitted and received carrier signals.

The transceiver/amplifier section **70** also serves as a receiver which receives an incoming carrier signal. This incoming signal is then demodulated within section **70**, the video and audio components of the incoming signal are separated, and then these separated signals are then sent to the digital signal processor **72** which performs video decompression. Then, the decompressed video signal is sent to the monitor **26** for viewing (if the video switch **37** is placed in that selected mode). The decompressed audio signal is sent to the amplifier **74**, and then to the speaker **76**.

FIG. **4** shows the transceiver/amplifier section **70** as being a cellular digital packet data system (CDPD) type transceiver. This particular transceiver/amplifier **70** could be the same as that disclosed in the U.S. Pat. No. 6,034,621. A cellular digital packet system is a wireless standard providing two-way, 19.2 kbps packet data transmission over existing cellular telephone channels.

The video switch **37** may simply be a momentary, spring loaded, push button-type switch. When the video switch **37** is not depressed, incoming video, which is received via the antenna **36**, is processed as discussed above in the transceiver/amplifier section **70** and digital signal processor **72**, and then sent to the monitor **26**. When the video switch **37** is depressed and held, the video signal produced from the camera module **10** is processed as discussed above, and ultimately sent to the monitor **26** for viewing by the user. An operator can cycle the switch **37** between the two positions in order to selectively choose whether to view incoming or outgoing video.

FIG. **5** illustrates a communications network which can be used by the invention. A communications network of this type is disclosed in the U.S. Pat. No. 6,034,621, and is discussed specifically therein at FIGS. 3 and 4 of that patent. FIG. **5** illustrates a CDPD base station **182** with a remote computer **188** utilizing a direct connection to the CDPD base station **182** via a modem **186** with a dial-up connection to the public switch telephone network (PSTN) **184**. The CDPD base station **182** includes an antenna **181**. The remote computer **188** can be a personal computer, a server, or any other well-known stand-alone computer.

Referring back to FIG. **4**, the computer processing and memory unit **82** which allows the PDA **22** to achieve basic

word processing, etc., includes a microprocessor **83**, RAM **84**, ROM **86**, and digital storage **88**. Digital storage **88** is provided for storing the formatted images taken by the camera module **10**. The RAM **84**, microprocessor **83**, and ROM **86** are conventional or standard components as found in existing PDAs. An input/output bus **89** is provided which allows video signals to be stored or otherwise manipulated within the computer processing and memory unit **82**. Accordingly, video taken by camera module **10** can be downloaded to digital storage **88**. Also, existing image data stored in digital storage **88** could be viewed on video monitor **26**.

FIGS. **6***a* and **6***b* illustrate another combination of the invention wherein the PDA **22** is simply combined with an externally mounted cellular telephone **190**. The cellular phone **190** is a commercially available cellular/wireless telephone. As shown, the telephone includes the standard keypad **194**, visual display **196**, and antennae **198**. The phone **190** is secured to the PDA **22** as by mounting means **192**, which is shown in the preferred embodiment as a piano-type hinge. Thus, the PDA is altered very simply by providing means by which a cellular telephone can be attached to the PDA. This enables the user to hold both the PDA and cellular telephone in one hand while manipulating the PDA or phone **190** as desired with the other hand. All of the telephone circuitry for phone **190** is housed within the phone itself, and there is no circuitry within the PDA which is used within the phone **190**.

The actual size of the phone **190** is smaller than the PDA **22**. However, in order to create a uniform edged combination, the phone **190** is housed in a larger housing **200** which essentially matches the dimensions of housing **24**. Additionally, a peripheral flange could be provided on the inner surface of housing **200** which comes into contact with housing **24** in the closed position of FIG. **6***a* which would prevent inadvertent activation of the control buttons on the PDA **22**.

FIG. **7** is a schematic diagram illustrating one way in which the imaging device **11** may be constructed. As illustrated, the image sensor **40** may include the timing and control circuits on the same planar structure. Power is supplied to image sensor **40** by power supply board **64**. The connection between image sensor **40** and board **64** may simply be a cable having two conductors therein, one for ground and another for transmitting the desired voltage. These are illustrated as conductors **44** and **46**. The output from image sensor **40** in the form of the pre-video signal is input to video processor board **50** by means of the conductor **48**. In the configuration of FIG. **7**, conductor **48** may simply be a 50 ohm conductor. Power and ground also are supplied to video processing board **50** by conductors **44** and **46** from power supply board **52**. The output signal from the video processor board **50** is in the form of the post-video signal and which may be carried by conductor **49** which can also be a 50 ohm conductor.

Although FIG. **7** illustrates the image sensor and the timing and control circuits being placed on the same circuit board or planar structure, it is possible to separate the timing and control circuits from the pixel array and place the timing and control circuits onto video processing board **50**. The advantage in placing the timing and control circuits on the same planar structure as the image sensor is that only three connections are required between image sensor **40** and the rest of the imaging device, namely, conductors **44**, **46** and **48**. Additionally, placing the timing and control circuits on the same planar structure with the pixel array results in the pre-video signal having less noise. Furthermore, the addition of the timing and control circuits to the same planar structure carrying the image sensor only adds a negligible amount of size to one dimension of the planar structure. If the pixel array is to be the only element on the planar structure, then additional connections must be made between the planar structure and the video processing board **50** in order to transmit the clock signals and other control signals to the pixel array. For example, a ribbon-type cable (not shown) or a plurality of 50 ohm coaxial cables (not shown) must be used in order to control the downloading of information from the pixel array. Each of these additional connections would be hard wired between the boards.

FIG. **7***a* is a more detailed schematic diagram of image sensor **40** which contains an array of pixels **90** and the timing and control circuits **92**. One example of a pixel array **90** which can be used within the invention is similar to that which is disclosed in U.S. Pat. No. 5,471,515 to Fossum, et al., said patent being incorporated by reference herein. More specifically, FIG. 3 of Fossum, et al. illustrates the circuitry which makes up each pixel in the array of pixels **90**. The array of pixels **90** as described in Fossum, et al. is an active pixel group with intra-pixel charged transfer. The image sensor made by the array of pixels is formed as a monolithic complementary metal oxide semiconductor (CMOS) integrated circuit which may be manufactured in an industry standard complementary metal oxide semiconductor process. The integrated circuit includes a focal plane array of pixel cells, each one of the cells including a photo gate overlying the substrate for accumulating the photo generated charges. In broader terms, as well understood by those skilled in the art, an image impinges upon the array of pixels, the image being in the form of photons which strike the photo diodes in the array of pixels. The photo diodes or photo detectors convert the photons into electrical energy or electrons which are stored in capacitors found in each pixel circuit. Each pixel circuit has its own amplifier which is controlled by the timing and control circuitry discussed below. The information or electrons stored in the capacitors is unloaded in the desired sequence and at a desired frequency, and then sent to the video processing board **50** for further processing.

Although the active pixel array disclosed in U.S. Pat. No. 5,471,515 is mentioned herein, it will be understood that the hybrid CCD/CMOS described above, or any other solid state imaging device may be used wherein timing and control circuits can be placed either on the same circuit board or planar structure with the pixel array, or may be separated and placed remotely. Furthermore, it will be clearly understood that the invention claimed herein is not specifically limited to an image sensor as disclosed in the U.S. Pat. No. 5,471,515, but encompasses any image sensor which may be configured for use in conjunction with the other processing circuitry which makes up the imaging device of this invention.

To summarize the different options available in terms of arrangement of the components of the imaging device **11**, the array of pixels **90** of the image sensor **40** may be placed alone on a first plane, or the timing and control circuitry **92** may be placed with the array of pixels **90** on the first plane. If the timing and control circuitry **92** is not placed with the array of pixels **90** on the first plane, the timing and control circuitry **92** may be placed by itself on a second plane, or the timing and control circuitry **92** may be placed on a second plane with some or all of the processing circuitry from video processing board **50**. The video processing board **50** itself may be placed on one or more planes on corresponding circuit boards containing video processing circuitry. FIG. **1***a*

illustrates a single video processor board **50** located directly behind image sensor **40**; however, it shall be understood that additional circuit boards containing additional circuitry may be placed behind the image sensor **40** and behind the video processing board **50**. Some or all of the video processing circuitry may be placed within the camera module **10** near the distal end thereof adjacent the image sensor **40**. Video processing circuitry which is not placed within the distal end of the camera module **10** may be placed within the housing **24** of the PDA. If video processing circuitry is placed near the distal end of the camera module **10**, it is preferable to arrange the video processing circuitry in a stacked relationship behind the image sensor **40**. Additionally, it is preferable to place the processing circuitry in a parallel arrangement with respect to image sensor **40** and to center such video processing circuitry along axis X—X in order to minimize the size of camera module **10**.

The timing and control circuits **92** are used to control the release of the image information or image signal stored in the pixel array. In the image sensor of Fossum, et al., the pixels are arranged in a plurality of rows and columns. The image information from each of the pixels is first consolidated in a row by row fashion, and is then downloaded from one or more columns which contain the consolidated information from the rows. As shown in FIG. 7*a,* the control of information consolidated from the rows is achieved by latches **94**, counter **96**, and decoder **98**. The operation of the latches, counter and decoder is similar to the operation of similar control circuitry found in other imaging devices. That is, a latch is a means of controlling the flow of electrons from each individual addressed pixel in the array of pixels. When a latch **94** is enabled, it will allow the transfer of electrons to the decoder **98**. The counter **96** is programmed to count a discrete amount of information based upon a clock input from the timing and control circuits **92**. When the counter **96** has reached its set point or overflows, the image information is allowed to pass through the latches **94** and be sent to the decoder **98** which places the consolidated information in a serial format. Once the decoder **98** has decoded the information and placed it in the serial format, then the row driver **100** accounts for the serial information from each row and enables each row to be downloaded by the column or columns. In short, the latches **94** will initially allow the information stored in each pixel to be accessed. The counter **96** then controls the amount of information flow based upon a desired time sequence. Once the counter has reached its set point, the decoder **98** then knows to take the information and place it in the serial format. The whole process is repeated, based upon the timing sequence that is programmed. When the row driver **100** has accounted for each of the rows, the row driver reads out each of the rows at the desired video rate.

The information released from the column or columns is also controlled by a series of latches **102**, a counter **104** and a decoder **106**. As with the information from the rows, the column information is also placed in a serial format which may then be sent to the video processing board **50**. This serial format of column information is the pre-video signal carried by conductor **48**. The column signal conditioner **108** places the column serial information in a manageable format in the form of desired voltage levels. In other words, the column signal conditioner **108** only accepts desired voltages from the downloaded column(s).

The clock input to the timing and control circuits **92** may simply be a quartz crystal timer. This clock input is divided into many other frequencies for use by the various counters. The run input to the timing and control circuit **92** may simply be an on/off control. The default input can allow one to input the pre-video signal to a video processor board which may run at a frequency of other than 30 hertz. The data input controls functions such as zoom. At least for a CMOS type active pixel array which can be accessed in a random manner, features such as zoom are easily manipulated by addressing only those pixels which locate a desired area of interest by the user.

A further discussion of the timing and control circuitry which may be used in conjunction with an active pixel array is disclosed in U.S. Pat. No. 5,471,515 and is also described in an article entitled "Active Pixel Image Sensor Integrated With Readout Circuits" appearing in *NASA Tech Briefs,* October 1996, pp. 38 and 39. This particular article is also incorporated by reference.

Once image sensor **40** has created the pre-video signal, it is sent to the video processing board **50** for further processing. At board **50**, as shown in FIG. 6*b,* the pre-video signal is passed through a series of filters. One common filter arrangement may include two low pass filters **114** and **116**, and a band pass filter **112**. The band pass filter only passes low frequency components of the signal. Once these low frequency components pass, they are then sent to detector **120** and white balance circuit **124**, the white balance circuit distinguishing between the colors of red and blue. The white balance circuit helps the imaging device set its normal, which is white. The portion of the signal passing through low pass filter **114** then travels through gain control **118** which reduces the magnitude or amplitude of this portion to a manageable level. The output from gain control **118** is then fed back to the white balance circuit **124**. The portion of the signal traveling through filter **116** is placed through the processor **122**. In the processor **122**, the portion of the signal carrying the luminance or non-chroma is separated and sent to the Y chroma mixer **132**. Any chroma portion of the signal is held in processor **122**.

Referring to the output of the white balance circuit **124**, this chroma portion of the signal is sent to a delay line **126** where the signal is then further reduced by switch **128**. The output of switch **128** is sent through a balanced modulator **130** and also to the Y chroma mixer **132** where the processed chroma portion of the signal is mixed with the processed non-chroma portion. Finally, the output from the Y chroma mixer **132** is sent to the NTSC/PAL encoder **134**, commonly known in the art as a "composite" encoder. The composite frequencies are added to the signal leaving the Y chroma mixer **132** in encoder **134** to produce the post-video signal which may be accepted by a television. Additionally, the signal from Y chroma mixer **132** is sent to the digital signal processor **72** so that images can be viewed on monitor **26**.

In addition to the functions described above that are achieved by the digital signal processor **72**, the processor **72** can also provide additional digital enhancements. Specifically, digital enhancement can sharpen or otherwise clarify the edges of an image viewed on a video screen which might normally be somewhat distorted. Additionally, selected background or foreground images may be removed thus only leaving the desired group of images.

In addition to digital enhancement, the digital signal processor **72** can include other circuitry which may further condition the signal received from board **50** so that it may be viewed in a desired format other than NTSC/PAL. One common encoder which can be used would be an RGB encoder. An RGB encoder separates the signal into the three primary colors (red, green and blue). A SVHS encoder (super video home system) encoder could also be added to

processor **72**. This type of encoder splits or separates the luminance portion of the signal and the chroma portion of the signal. Some observers believe that a more clear signal is input to the video device by such a separation, which in turn results in a more clear video image viewed on the video device. Another example of an encoder which could be added to processor **72** includes a VGA compatible encoder, which enables the video signal to be viewed on a standard VGA monitor which is common to many computer monitors.

One difference between the arrangement of image sensor **40** and the outputs found in FIG. 3 of the Fossum, et al. patent is that in lieu of providing two analog outputs [namely, VS out (signal) and VR out (reset)], the reset function takes place in the timing and control circuitry **92**. Accordingly, the pre-video signal only requires one conductor **48**.

FIGS. **8***a*–**8***e* illustrate in more detail one example of circuitry which may be used in the video processing board **50** in order to produce a post-video signal which may be directly accepted by a NTSC/PAL compatible video device such as a television. The circuitry disclosed in FIGS. **8***a*–**8***e* is very similar to circuitry which is found in a miniature quarter-inch Panasonic camera, Model KS-162. It will be understood by those skilled in the art that the particular arrangement of elements found in FIGS. **8***a*–**8***e* are only exemplary of the type of video processing circuitry which may be incorporated in order to take the pre-video signal and condition it to be received by a desired video device.

As shown in FIG. **8***a,* 5 volt power is provided along with a ground by conductors **44** and **46** to board **50**. The pre-video signal carried by conductor **48** is buffered at buffer **137** and then is transferred to amplifying group **138**. Amplifying group **138** amplifies the signal to a usable level as well as achieving impedance matching for the remaining circuitry.

The next major element is the automatic gain control **140** shown in FIG. **8***b.* Automatic gain control **140** automatically controls the signal from amplifying group **138** to an acceptable level and also adds other characteristics to the signal as discussed below. More specifically, automatic gain control **140** conditions the signal based upon inputs from a 12 channel digital to analog converter **141**. Converter **141** retrieves stored information from EEPROM (electrically erasable programmable read only memory) **143**. EEPROM **143** is a non-volatile memory element which may store user information, for example, settings for color, tint, balance and the like. Thus, automatic gain control **140** changes the texture or visual characteristics based upon user inputs. Housing **24** could also include buttons for controlling the image viewed on monitor **26** such as a gain control **140**. The signal leaving the automatic gain control **140** is an analog signal until being converted by analog to digital converter **142**.

Digital signal processor **144** of FIG. **8***c* further processes the converted signal into a serial type digital signal. One function of the microprocessor **146** is to control the manner in which digital signal processor **144** sorts the digital signals emanating from converter **142**. Microprocessor **146** also controls analog to digital converter **142** in terms of when it is activated, when it accepts data, when to release data, and the rate at which data should be released. Microprocessor **146** may also control other functions of the imaging device such as white balance. The microprocessor **146** may selectively receive the information stored in the EEPROM **143** and carry out its various commands to further control the other elements within the circuitry.

After the signal is processed by digital signal processor **144**, the signal is sent to digital encoder **148** illustrated in FIG. **8***d.* Some of the more important functions of digital encoder **148** are to encode the digital signal with synchronization, modulated chroma, blanking, horizontal drive, and the other components necessary so that the signal may be placed in a condition for reception by a video device such as a television monitor. As also illustrated in FIG. **8***d,* once the signal has passed through digital encoder **148**, the signal is reconverted into an analog signal through digital to analog converter **150**.

This reconverted analog signal is then buffered at buffers **151** and then sent to amplifier group **152** of FIG. **8***e* which amplifies the signal so that it is readily accepted by a desired video device. Specifically, as shown in FIG. **8***e,* one SVHS outlet is provided at **160**, and two composite or NTSC outlets are provided at **162** and **164**, respectively.

From the foregoing, it is apparent that an entire imaging device may be incorporated within the distal tip of the camera module, or may have some elements of the imaging device being placed in the housing of the PDA. Based upon the type of image sensor used, the profile area of the imaging device may be made small enough to be placed into a camera module which has a very small diameter.

This invention has been described in detail with reference to particular embodiments thereof, but it will be understood that various other modifications can be effected within the spirit and scope of this invention.

What is claimed is:

1. In a PDA having capability to transmit data between a personal computer connected to a communications network, the improvement comprising:

a video system integral with said PDA for receiving and transmitting video images, and for viewing said video images, said video system comprising;

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of CMOS pixels for timing and control of said array of CMOS pixels, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically coupled to said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;

a video view screen attached to said PDA for viewing said video images, said video view screen communicating with said first circuit board, and displaying video images processed by said first circuit board.

2. A device, as claimed in claim **1**, wherein:

said first circuit board is placed adjacent said image sensor within said camera module.

3. A device, as claimed in claim **1**, wherein:

said first circuit board is remote from said image sensor and placed within a housing of said PDA.

4. A device, as claimed in claim **1**, wherein:

said image sensor defines a profile area in said first plane, and said first circuit board is positioned in longitudinal alignment with said image sensor such that said first circuit board does not extend substantially beyond said profile area.

5. A device, as claimed in claim **1**, further including:

a second circuit board electrically coupled with said first circuit board and said image sensor for further process-

ing said pre-video signal, said second board being placed adjacent said first circuit board within said camera module.

6. A device, as claimed in claim **1**, wherein:

said first and second planes are offset from and substantially parallel to one another.

7. A device, as claimed in claim **5**, wherein:

said second circuit board lies in a third plane which is offset from and extends substantially parallel to said first and second planes.

8. A device, as claimed in claim **5**, wherein:

said second circuit board includes means for digital signal processing enabling the pre-video signal conditioned by said first circuit board to be viewed by said video view screen.

9. A device, as claimed in claim **1**, wherein:

said first circuit board converts said pre-video signal to a post-video signal for direct reception by a remote video device, said post-video signal being of a format selected from the group consisting of a NTSC/PAL video signal and a VGA video signal.

10. A device, as claimed in claim **1**, wherein:

said array of CMOS pixels includes an array of passive CMOS pixels, wherein individual passive CMOS pixels of said array of passive CMOS pixels each include a photo diode for producing photoelectrically generated signals, and an access transistor communicating with said photo diode to control the release of photoelectrically generated signals.

11. A device, as claimed in claim **1**, wherein:

individual pixels within said array of CMOS pixels each include an amplifier.

12. A device, as claimed in claim **1**, further including:

a retractable cable interconnecting said camera module to said PDA, said retractable cable enabling said camera module to be pulled away from said PDA for selective taking of images by said camera module, and allowing said camera module to be stored within said PDA by retracting said cable and securing said camera module within said PDA.

13. A device, as claimed in claim **1**, wherein:

said PDA includes a text screen mounted therein for viewing text which is manipulated by a user.

14. A device as claimed in claim **1**, further including:

a wireless telephone attached to said PDA.

15. A device, as claimed in claim **1**, further including:

a remote video device electrically coupled to said video system for further viewing said video images.

16. A device, as claimed in claim **15**, wherein:

said remote video device is selected from the group consisting of a television and a computer monitor.

17. In a PDA having capability to transmit data between a computer connected to a communications network, the PDA having a housing, and a video view screen for viewing the data which includes video signals, the improvement comprising:

a camera module for taking video images, said camera module communicating with circuitry within said PDA enabling viewing on said video view screen and enabling video signals to be transmitted from said camera module to said computer, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of said CMOS pixels for timing and control of said array of CMOS pixels, said image sensor producing a pre-video signal; and

a first circuit board electrically connected to said image sensor and separated from said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format.

18. A device, as claimed in claim **17**, wherein:

said first circuit board is placed adjacent said image sensor within said camera module.

19. A device, as claimed in claim **17**, wherein:

said first circuit board is placed within said housing of said PDA.

20. A device, as claimed in claim **17**, wherein:

said image sensor defines a profile area in said first plane, and said first circuit board is positioned in longitudinal alignment with said image sensor such that said first circuit board does not extend substantially beyond said profile area.

21. A device, as claimed in claim **17**, further including:

a second circuit board electrically coupled with said first circuit board and said image sensor for further processing said pre-video signal, said second board being placed adjacent said first circuit board within said camera module.

22. A device, as claimed in claim **17**, wherein:

said first and second planes are offset from and substantially parallel to one another.

23. A device, as claimed in claim **17**, wherein:

said second circuit board lies in a third plane which is offset from and extends substantially parallel to said first and second planes.

24. A device, as claimed in claim **17**, wherein:

said second circuit board includes means for digital signal processing enabling the pre-video signal conditioned by said first circuit board to be viewed by said video view screen.

25. A device, as claimed in claim **17**, wherein:

said first circuit board converts said pre-video signal to a post video signal for direct reception by a remote video device, said post-video signal being of a format selected from the group consisting of a NTSC/PAL video signal and a VGA video signal.

26. A device, as claimed in claim **17**, wherein:

said array of CMOS pixels includes an array of passive CMOS pixels, wherein individual passive CMOS pixels of said array of passive CMOS pixels each include a photo diode for producing photoelectrically generated signals, and an access transistor communicating with said photo diode to control the release of photoelectrically generated signals.

27. A device, as claimed in claim **17**, wherein:

individual pixels within said array of CMOS pixels each include an amplifier.

28. A device, as claimed in claim **17**, further including:

a retractable cable interconnecting said camera module to said PDA, said retractable cable enabling said camera module to be pulled away from said PDA for selective taking of images by said camera module, and allowing said camera module to be stored within said PDA by retracting said cable and securing said camera module within said PDA.

29. A device, as claimed in claim **17**, wherein:

said PDA includes a command screen mounted therein for executing commands directed by a user.

30. A device as claimed in claim 17, further including:

a wireless telephone attached to said PDA.

31. A device, as claimed in claim 17, further including:

a remote video device electrically coupled to said PDA for further viewing said video images.

32. A device, as claimed in claim 31, wherein:

said remote video device is selected from the group consisting of a television and a computer monitor.

33. A PDA having capability for receiving and transmitting video and audio images between the PDA and a personal computer connected to a communications network, said PDA comprising:

an image sensor lying in a first plane, and an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of CMOS pixels for timing and control of said array of CMOS pixels, said image sensor producing a pre-video signal;

a first circuit board electrically communicating with said image sensor and separated from said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;

a camera module housing said image sensor;

a transceiver/amplifier section electrically coupled to said first circuit board for transmitting, receiving, and amplifying video and audio signals;

a digital signal processor electrically coupled to said first circuit board and said transceiver/amplifier section, said digital signal processor further conditioning said pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals from said transceiver/amplifier section;

a microphone electrically communicating with said digital signal processor for recording and receiving audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video view screen attached to said PDA, said video view screen for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section;

a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video view screen; and

a power supply mounted to said PDA for providing power thereto.

34. A device, as claimed in claim 33, wherein:

said first circuit board is placed adjacent said image sensor within said camera module.

35. A device, as claimed in claim 33, wherein:

said first circuit board is remote from said image sensor and placed within a housing of said PDA.

36. A device, as claimed in claim 33, wherein:

said image sensor defines a profile area in said first plane, and said first circuit board is positioned in longitudinal alignment with said image sensor such that said first circuit board does not extend substantially beyond said profile area.

37. A device, as claimed in claim 33, further including:

a second circuit board electrically coupled with said first circuit board and said image sensor for further processing said pre-video signal, said second board being placed adjacent said first circuit board.

38. A device, as claimed in claim 33, wherein:

said first and second planes are offset from and substantially parallel to one another.

39. A device, as claimed in claim 37, wherein:

said second circuit board lies in a third plane which is offset from and extends substantially parallel to said first and second planes.

40. A device, as claimed in claim 37, wherein:

said second circuit board includes means for digital signal processing enabling the pre-video signal conditioned by said first circuit board to be viewed by said video view screen.

41. A device, as claimed in claim 33, wherein:

said first circuit board converts said pre-video signal to a post-video signal for direct reception by a remote video device, said post-video signal being of a format selected from the group consisting of a NTSC/PAL video signal and a VGA video signal.

42. A device, as claimed in claim 33, wherein:

said array of CMOS pixels includes an array of passive CMOS pixels, wherein individual passive CMOS pixels of said array of passive CMOS pixels each include a photo diode for producing photoelectrically generated signals, and an access transistor communicating with said photo diode to control the release of photoelectrically generated signals.

43. A device, as claimed in claim 33, wherein:

individual pixels within said array of CMOS pixels each include an amplifier.

44. A device, as claimed in claim 33, further including:

a retractable cable interconnecting said imaging device to said PDA, said retractable cable enabling said imaging device to be pulled away from said PDA for selective taking of images by said imaging device, and allowing said imaging device to be stored within said PDA by retracting said cable and securing said camera module within said PDA.

45. A device, as claimed in claim 33, wherein:

said PDA includes a text screen mounted therein for viewing text which is manipulated buy a user.

46. A device as claimed in claim 33, further including:

a wireless telephone attached to said PDA.

47. A device, as claimed in claim 33, further including:

a remote video device electrically coupled to said video system for further viewing said video image.

48. A device, as claimed in claim 47, wherein:

said remote video device is selected from the group consisting of a television and a computer monitor.

49. In a PDA having capability to transmit data between a personal computer connected to a communications network, the improvement comprising:

a video system integral with said PDA for receiving and transmitting video images, and for viewing said images, said video system comprising:

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically coupled to said image sensor, said first circuit board including circuitry means for timing and control of said array of CMOS pixels and circuitry means for processing and converting said pre-video signal to a desired video format; and

a video view screen attached to said PDA for viewing said video images, said video view screen communicating with said first circuit board.

50. A device, as claimed in claim 49, wherein:

said first circuit board is placed adjacent to said image sensor and within said camera module.

51. A device, as claimed in claim 49, wherein:

said first circuit board is remote from said image sensor and placed within a housing of said PDA.

52. In a PDA having capability to transmit data between a personal computer connected to a communications network, the improvement comprising:

a video system integral with said PDA for receiving and transmitting video images, and for viewing said images, said video system comprising:

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, circuitry means electrically coupled to said array of CMOS pixels for timing and control of said array of CMOS pixels, said circuitry means for timing and control being placed remote from said array of CMOS pixels on a second plane, said image sensor producing a pre-video signal, a first circuit board lying in a third plane and electrically coupled to said image sensor, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format; and

a video view screen attached to said PDA for viewing said video images, said video view screen communicating with said first circuit board, and displaying video images processed by said first circuit board.

53. A device, as claimed in claim 52, wherein:

said circuitry means for timing and control is placed adjacent to said image sensor in said camera module.

54. A device, as claimed in claim 52, wherein:

said circuitry means for timing and control is placed within a housing of the PDA.

55. In a PDA having capability to transmit data between a personal computer connected to a communications network, the PDA including a video view screen for viewing video images, the improvement comprising:

a camera module for taking video images, said camera module communicating with circuitry within said PDA enabling viewing on said video view screen and enabling video signals to be transmitted from said camera module to the personal computer, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically connected to said image sensor, said first circuit board including circuitry means for timing and control of said array of CMOS pixels and circuitry means for processing and converting said pre-video signal to a desired video format.

56. A device, as claimed in claim 55, wherein:

said first circuit board is placed adjacent said image sensor within said camera module.

57. A device, as claimed in claim 55, wherein:

said first circuit board is placed within a housing of said PDA.

58. In a PDA having capability to transmit data between a personal computer connected to a communications network, the PDA including a video view screen for viewing the video images, the improvement comprising:

a camera module for taking video images, said camera module communicating with circuitry within said PDA enabling viewing of said video images on said PDA and enabling video signals to be transmitted from said camera module to the personal computer, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of said CMOS pixels for timing and control of said array of CMOS pixels, said circuitry means for timing and control placed remote from said array of CMOS pixels on a second plane, said image sensor producing a pre-video signal, a first circuit board electrically connected to said image sensor and lying in a third plane, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format.

59. A device, as claimed in claim 58, wherein:

said circuitry means for timing and control is placed adjacent to said image sensor in said camera module.

60. A device, as claimed in claim 58, wherein:

said circuitry means for timing and control is placed within a housing of said PDA.

61. A PDA having capability for receiving and transmitting video and audio images between the PDA and a personal computer connected to a communications network, said PDA comprising:

an image sensor lying in a first plane including an array of CMOS pixels for receiving images thereon, said image sensor producing a pre-video signal;

a first circuit board electrically communicating with said image sensor and separated from said image sensor, said first circuit board including circuitry means for timing and control of said array of CMOS pixels and circuitry means for processing and converting said pre-video signal to a desired video format;

a camera module housing said image sensor;

a transceiver/amplifier section electrically coupled to said first circuit board for transmitting, receiving, and amplifying video and audio signals;

a digital signal processor electrically coupled to said first circuit board and said transceiver/amplifier section, said digital signal processor further conditioning said pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals from said transceiver/amplifier section;

a microphone electrically communicating with said digital signal processor for recording and receiving audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video view screen attached to said PDA, said video view screen for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section;

a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video view screen; and

a power supply mounted to said PDA for providing power thereto.

62. A device, as claimed in claim 61, wherein:

said first circuit board is placed adjacent to said image sensor and within said camera module.

63. A device, as claimed in claim 61, wherein:

said first circuit board is remote from said image sensor, and placed within a housing of said PDA.

64. A PDA having capability for receiving and transmitting video and audio images between the PDA and a personal computer connected to a communications network, said PDA comprising:

an image sensor lying in a first plane, and an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of CMOS pixels for timing and control of said array of CMOS pixels, said circuitry means for timing and control being placed remote from said array of CMOS pixels on a second plane, said image sensor producing a pre-video signal;

a first circuit board electrically coupled with said image sensor and lying in a third plane, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format;

a camera module housing said image sensor;

a transceiver/amplifier section electrically coupled to said first circuit board for transmitting, receiving, and amplifying video and audio signals;

a digital signal processor electrically coupled to said first circuit board and said transceiver/amplifier section, said digital signal processor further conditioning said pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals from said transceiver/amplifier section;

a microphone electrically communicating with said digital signal processor for recording and receiving audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video view screen attached to said PDA, said video view screen for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section;

a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video view screen; and

a power supply mounted to said PDA for providing power thereto.

65. A device, as claimed in claim 64, wherein:

said circuitry means for timing and control is placed adjacent to said image sensor in said camera module.

66. A device, as claimed in claim 65, wherein:

said circuitry means for timing and control is placed within a housing of said PDA.

67. In a method for conducting video conferencing communications through connection with a communications network, the improvement comprising the steps of:

providing a camera module having an image sensor housed therein;

providing a flexible cable for interconnecting the camera module to a PDA;

displacing the camera module away from the PDA;

pointing the camera module at a targeted object; and

taking video images of the targeted object by the camera module for viewing on the PDA, and for transmission of the video images to the communications network.

68. A method, as claimed in claim 67, further comprising the steps of:

selectively extending and selectively retracting the cable, enabling the camera module to be pointed in a desired direction toward the targeted object.

69. A method, as claimed in claim 67, wherein:

said image sensor includes a CMOS pixel array.

70. In a PDA having capability for data exchange between a personal computer connected to a communications network, the improvement comprising:

a camera module housing an image sensor therein, said camera module for producing video images of a targeted object;

means for interconnecting said camera module to said PDA, said means for interconnecting including a flexible cable enabling said camera module to be selectively displaced at a location remote from said PDA; and

a video view screen attached to said PDA for selectively viewing video images taken by said camera module, and for selectively viewing incoming video images received from the personal computer connected to the communications network.

71. A device, as claimed in claim 70, wherein:

said PDA includes a housing, and an opening for receiving said camera module so as to place said camera module in a stored position.

72. In a PDA having a housing and a video view screen for viewing video images, the improvement comprising:

a camera module housing an image sensor therein, said camera module for producing video images of a targeted object; and

means for interconnecting said camera module to said PDA, said means for interconnecting including a flexible cable enabling said camera module to be selectively displaced at a location remote from said PDA.

73. A device, as claimed in claim 72, wherein:

said PDA includes an opening in said housing for receiving said camera module so as to place said camera module in a stored position.

74. In a PDA, the improvement comprising:

a camera module housing an image sensor therein;

circuitry means coupled to said image sensor for timing and control of said image sensor;

circuitry means for processing images taken by said image sensor to create video signals of a desired video format;

means for interconnecting said camera module to a housing of said PDA, said means for interconnecting including a flexible connection enabling said camera module to be selectively displaced at multiple angles from said housing by the user for pointing the camera module at a targeted object, and enabling said camera module to be retracted for movement back to said housing.

75. A device, as claimed in claim 74, wherein:

said PDA includes an opening in said housing for receiving said camera module so as to place said camera module in a stored position.

* * * * *

US006452626B1

(12) **United States Patent**
Adair et al.

(10) **Patent No.: US 6,452,626 B1**
(45) **Date of Patent: Sep. 17, 2002**

(54) **COMMUNICATION DEVICES INCORPORATING REDUCED AREA IMAGING DEVICES**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 59 days.

(21) Appl. No.: **09/613,027**

(22) Filed: **Jul. 10, 2000**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/496,312, filed on Feb. 1, 2000, which is a continuation of application No. 09/175,685, filed on Oct. 20, 1998, now Pat. No. 6,043,839, which is a continuation-in-part of application No. 08/944,322, filed on Oct. 6, 1997, now Pat. No. 5,929,901.

(51) **Int. Cl.**[7] **H04N 7/18**; H04Q 7/32

(52) **U.S. Cl.** **348/158**; 348/376; 455/90; 455/566; 455/556; 455/557

(58) **Field of Search** 455/566, 556, 455/557, 575, 90; 348/60–80, 376, 158

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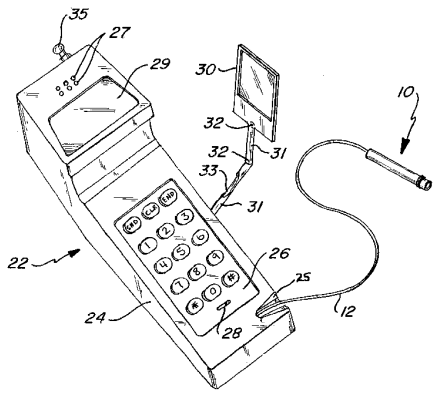
Primary Examiner—Andy Rao
(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

A reduced area imaging device is provided for use with a communication device, such as a wireless/cellular phone. In one configuration of the imaging device, the image sensor is placed remote from the remaining image processing circuitry. In a second configuration, all of the image processing circuitry to include the image sensor is placed in a stacked fashion near the same location. In the first configuration, the entire imaging device can be placed at the distal end of a camera module. In a second configuration, the image sensor is remote from the remaining image processing circuitry wherein available space within the phone is used to house the remaining circuitry. In any of the embodiments, the image sensor may be placed alone on a first circuit board, or timing and control circuits may be included on the first circuit board containing the image sensor. One or more video processing boards can be stacked in a longitudinal fashion with respect to the first board, or the video processing boards may be placed within the housing of the communication device. The communication device includes a miniature LCD-type monitor which is capable of viewing not only the images taken by the camera module, but also can show incoming video images. The camera module is of such small size that it can be easily stored within the housing of the communication device, and may be attached thereto as by a small retractable cable. Having a tethered camera module allows it to be pointed at any desired object within sight of the user, and without having to actually point or move the phone housing in order to take an image.

74 Claims, 12 Drawing Sheets



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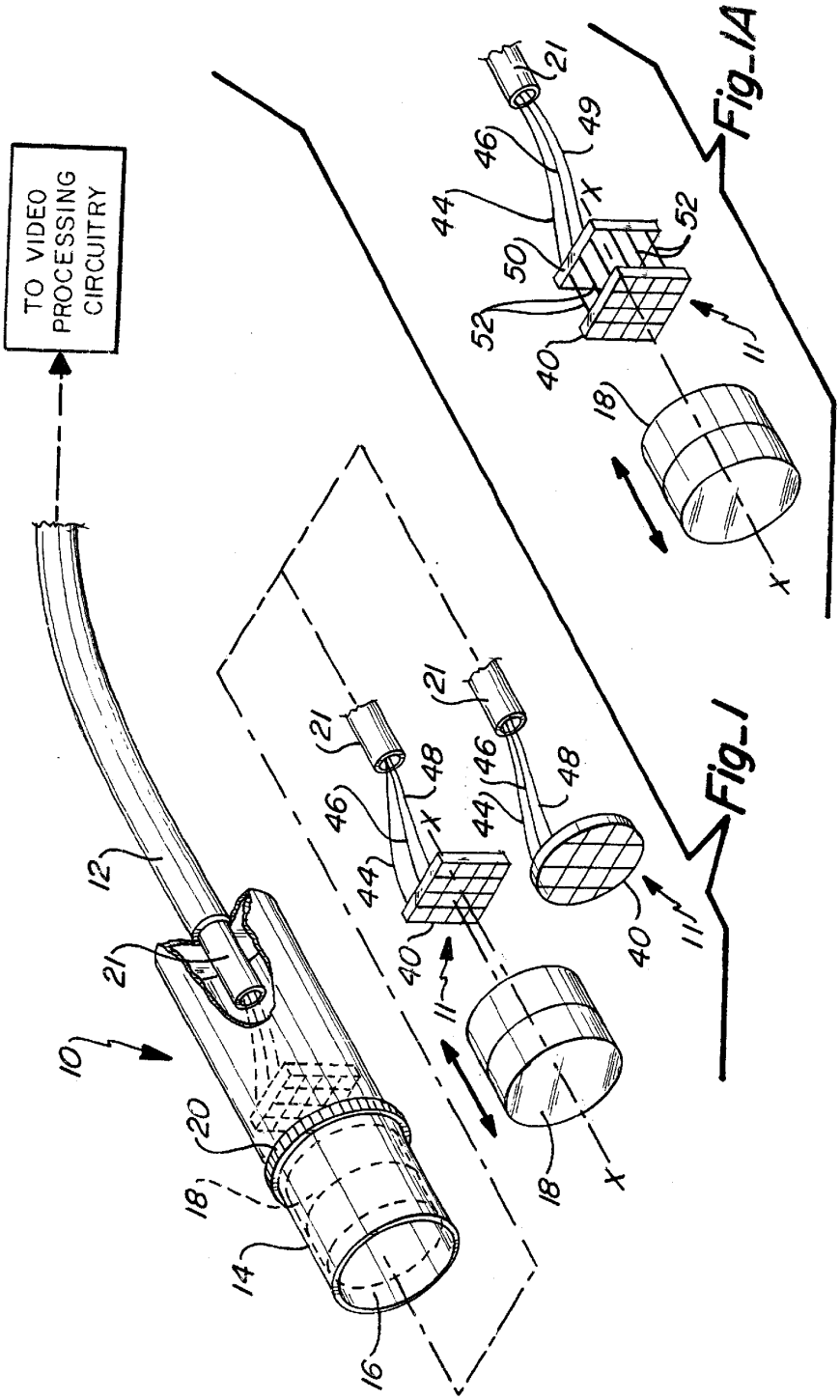
TO VIDEO PROCESSING CIRCUITRY
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X
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Fig_1A

Fig_1

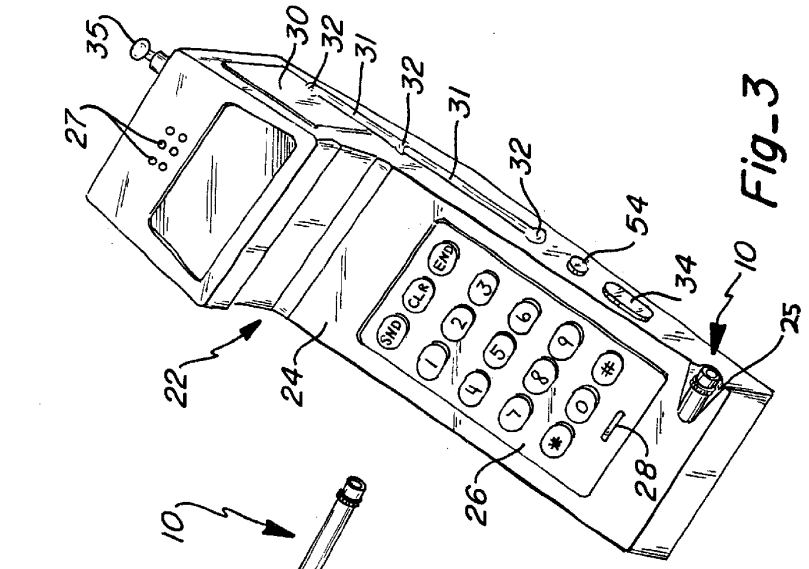
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Fig_3

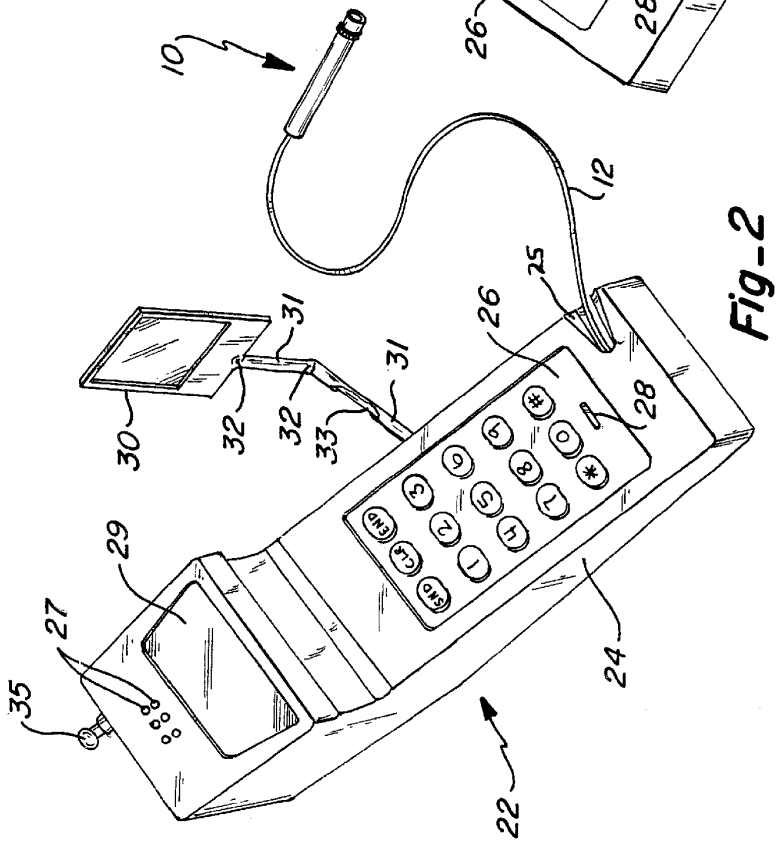
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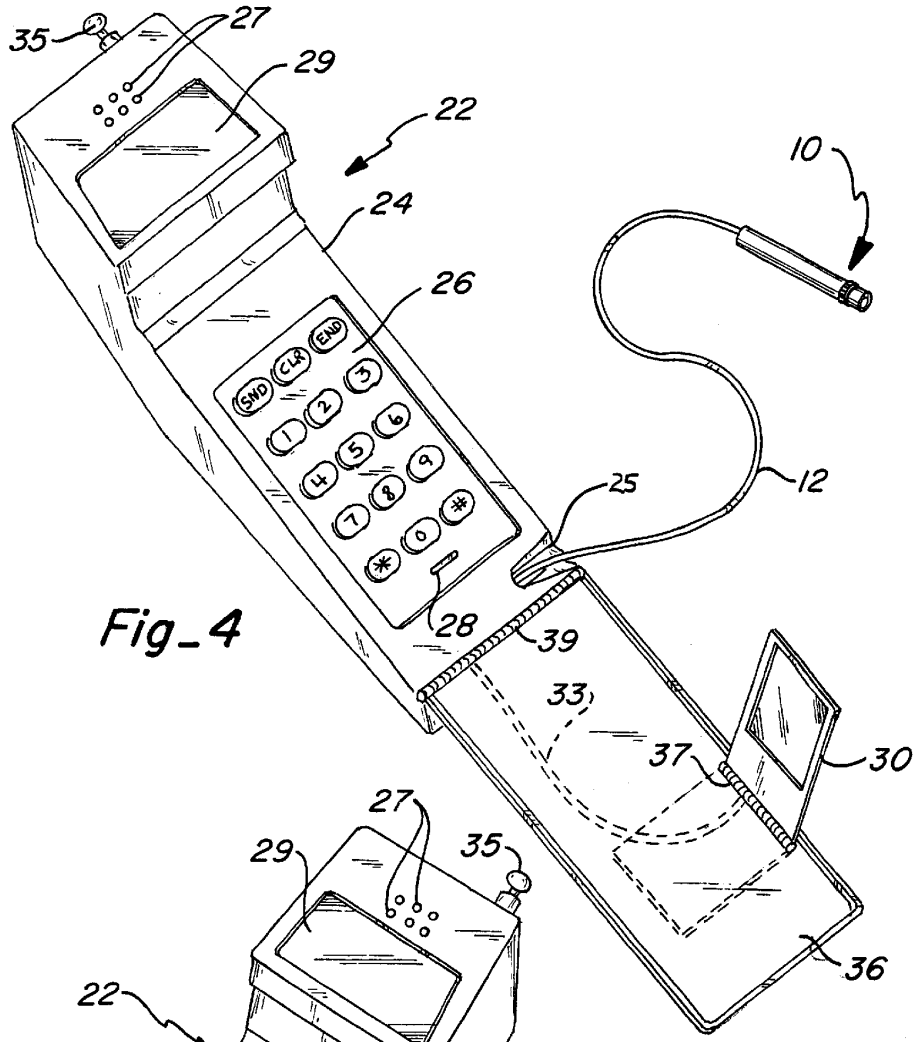
Fig_2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SND
CLR
END
1
2
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*
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#
25
12
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30
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Fig_4

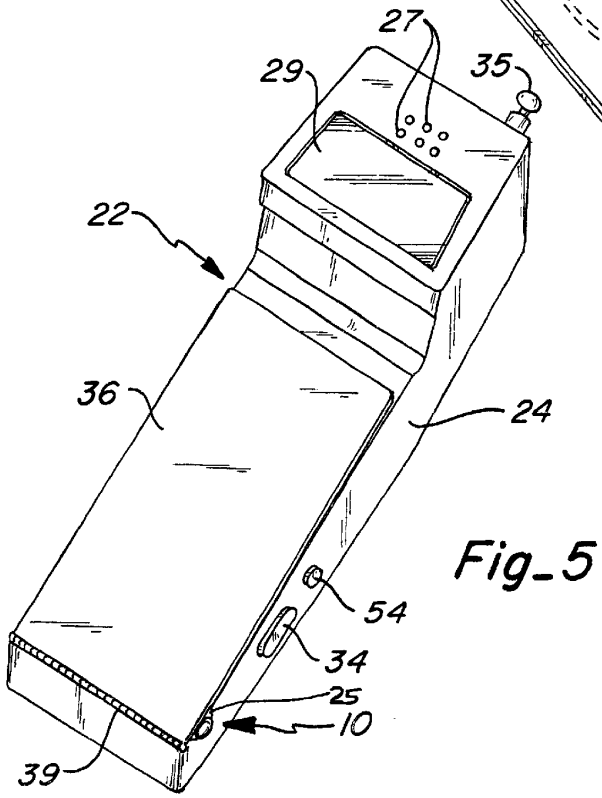
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Fig_5

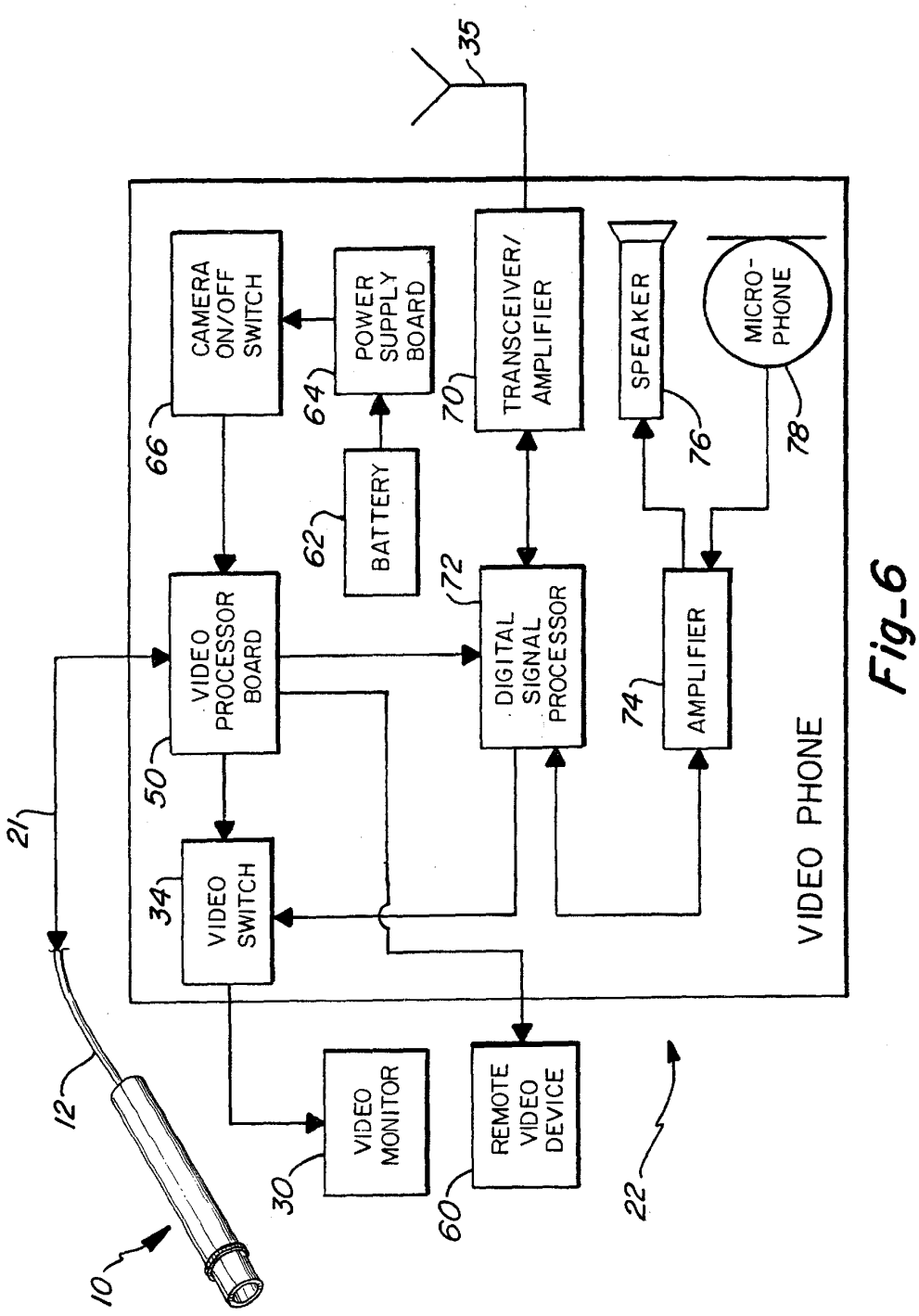
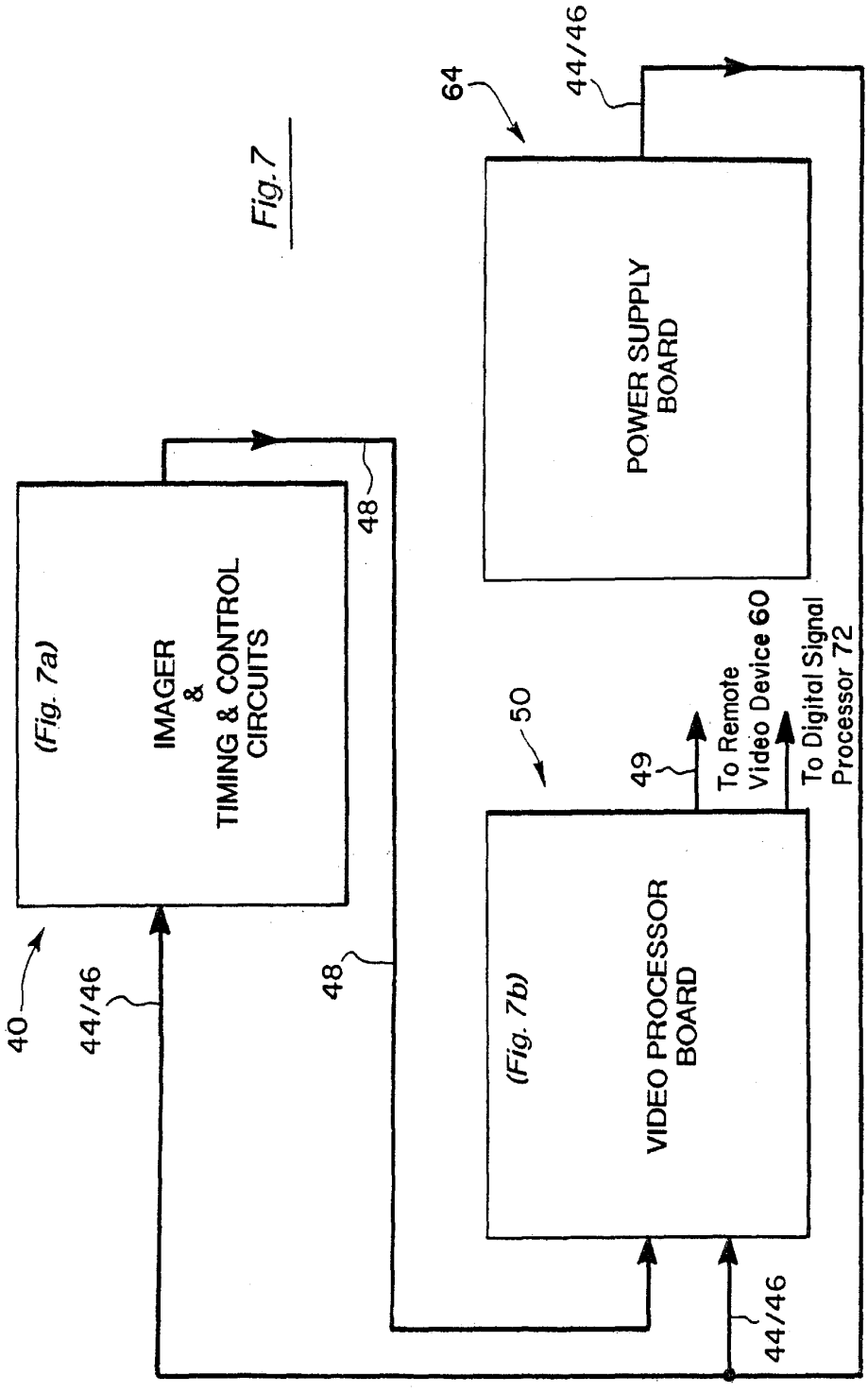
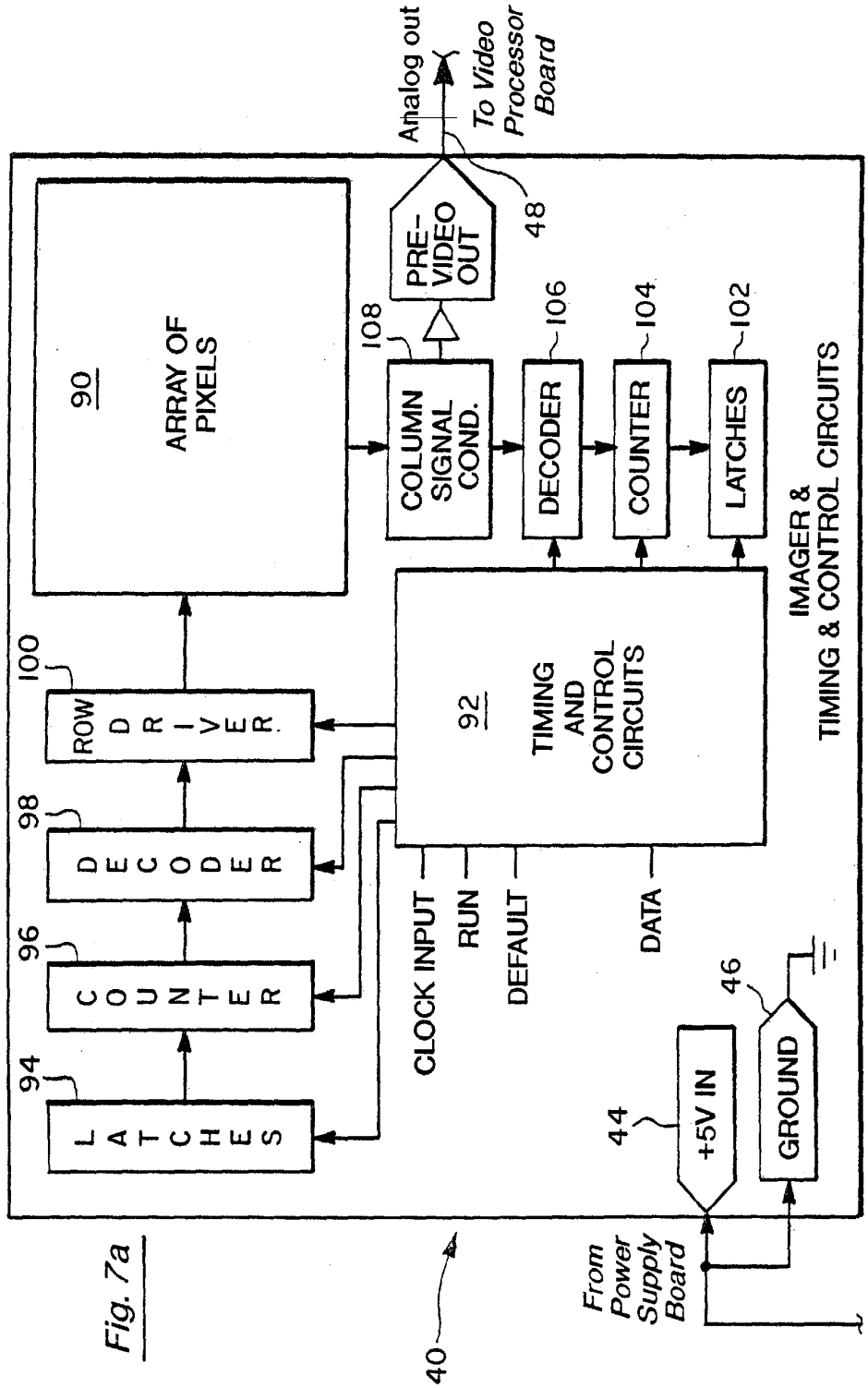

35
CAMERA ON/OFF SWITCH
66
POWER SUPPLY BOARD
64
TRANSCEIVER/ AMPLIFIER
70
SPEAKER
76
MICRO-PHONE
78
BATTERY
62
VIDEO PROCESSOR BOARD
50
DIGITAL SIGNAL PROCESSOR
72
AMPLIFIER
74
VIDEO PHONE
21
VIDEO SWITCH
34
12
VIDEO MONITOR
30
REMOTE VIDEO DEVICE
60
22
10

Fig_6

Fig. 7


64
44/46
POWER SUPPLY BOARD
48
(Fig. 7a)
IMAGER & TIMING & CONTROL CIRCUITS
50
49
To Remote Video Device 60
To Digital Signal Processor 72
40
44/46
48
(Fig. 7b)
VIDEO PROCESSOR BOARD
44/46


Analog out
To Video Processor Board
48
PRE-VIDEO OUT
108
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ARRAY OF PIXELS
COLUMN SIGNAL COND.
106
DECODER
104
COUNTER
102
LATCHES
IMAGER & TIMING & CONTROL CIRCUITS
100
ROW DRIVER
92
TIMING AND CONTROL CIRCUITS
98
DECODER
96
COUNTER
94
LATCHES
CLOCK INPUT
RUN
DEFAULT
DATA
46
44
+5V IN
GROUND
From Power Supply Board
40

Fig. 7a

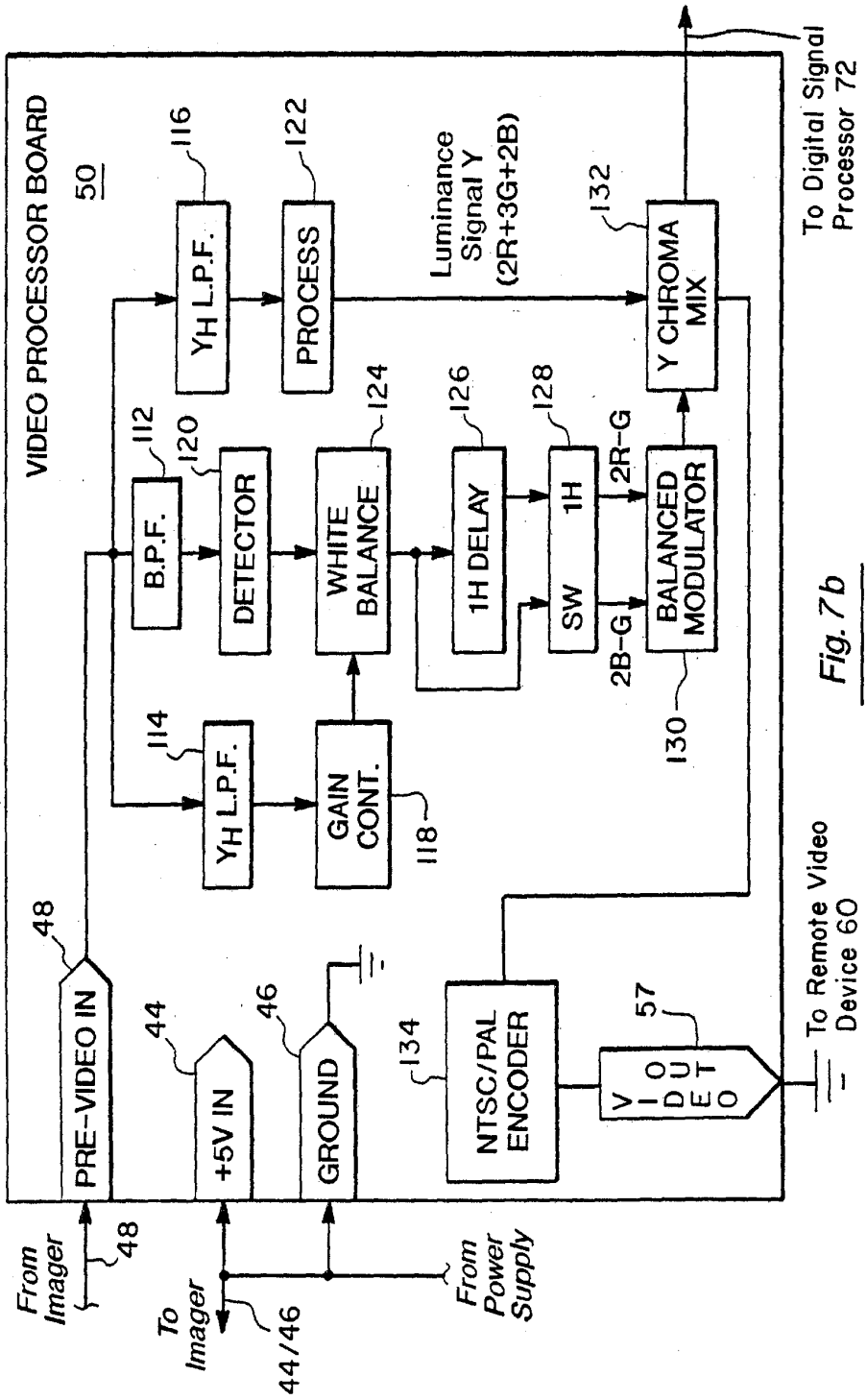
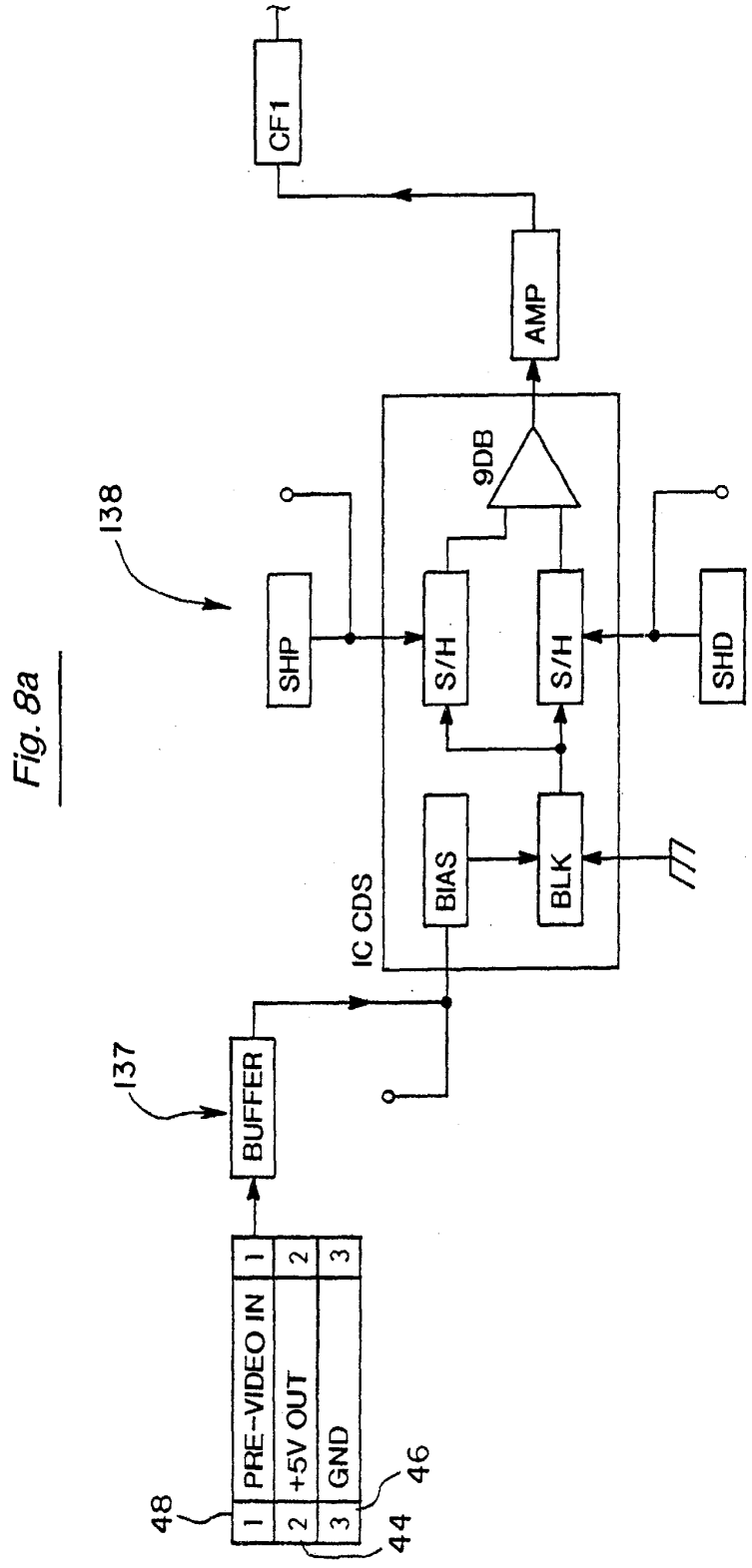

VIDEO PROCESSOR BOARD
50
PRE-VIDEO IN
48
+5V IN
44
GROUND
46
B.P.F.
112
DETECTOR
120
YH L.P.F.
116
PROCESS
122
Luminance Signal Y (2R+3G+2B)
Y CHROMA MIX
132
To Digital Signal Processor 72
WHITE BALANCE
124
1H DELAY
126
SW 1H
128
2R-G
2B-G
BALANCED MODULATOR
130
YH L.P.F.
114
GAIN CONT.
118
NTSC/PAL ENCODER
134
VIDEO OUT
57
To Remote Video Device 60
From Imager
48
To Imager
44/46
From Power Supply

Fig. 7b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SHP
S/H
S/H
SHD
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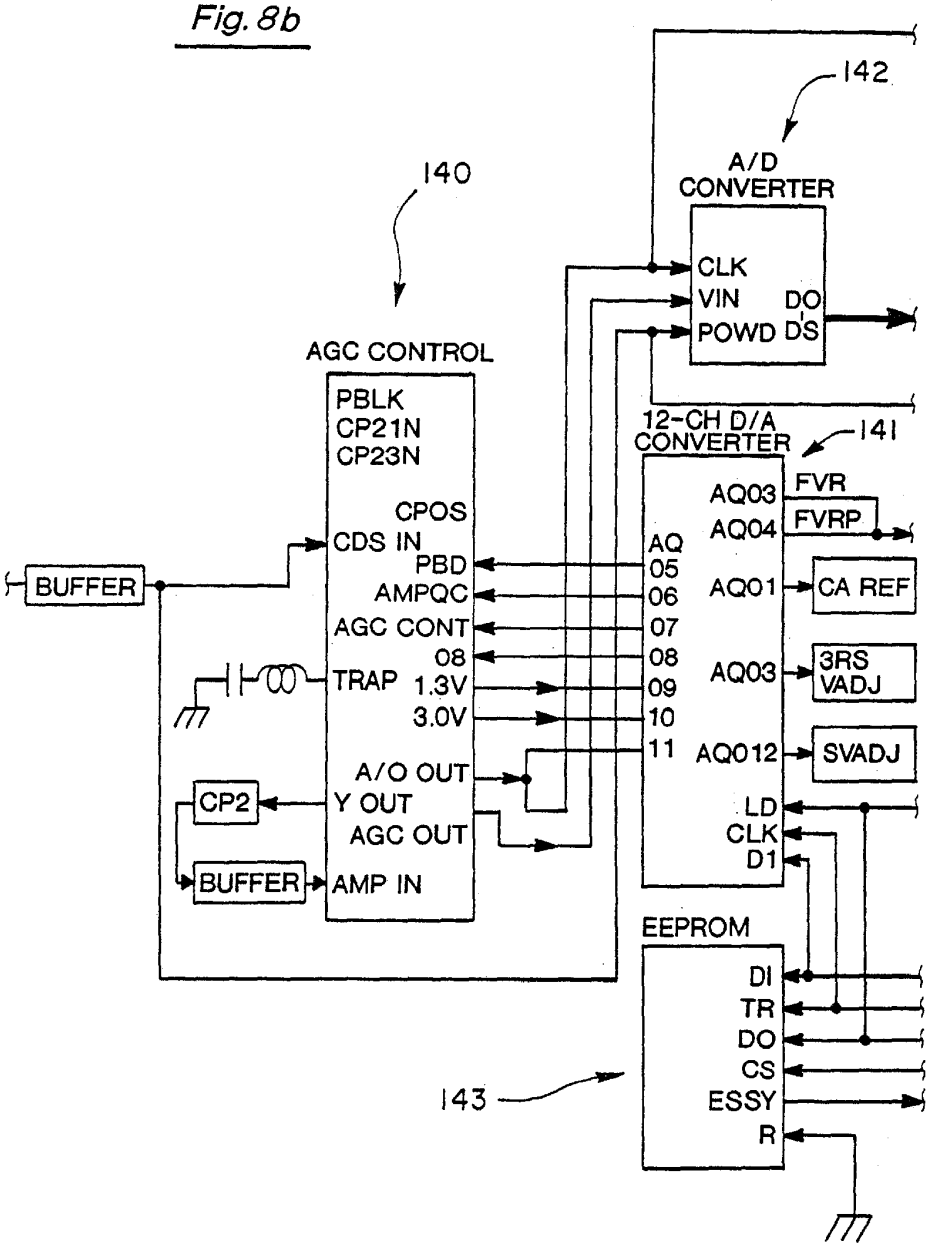
PRE-VIDEO IN
+5V OUT
GND
48
46
44

Fig. 8a

Fig. 8b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CP23N
CPOS
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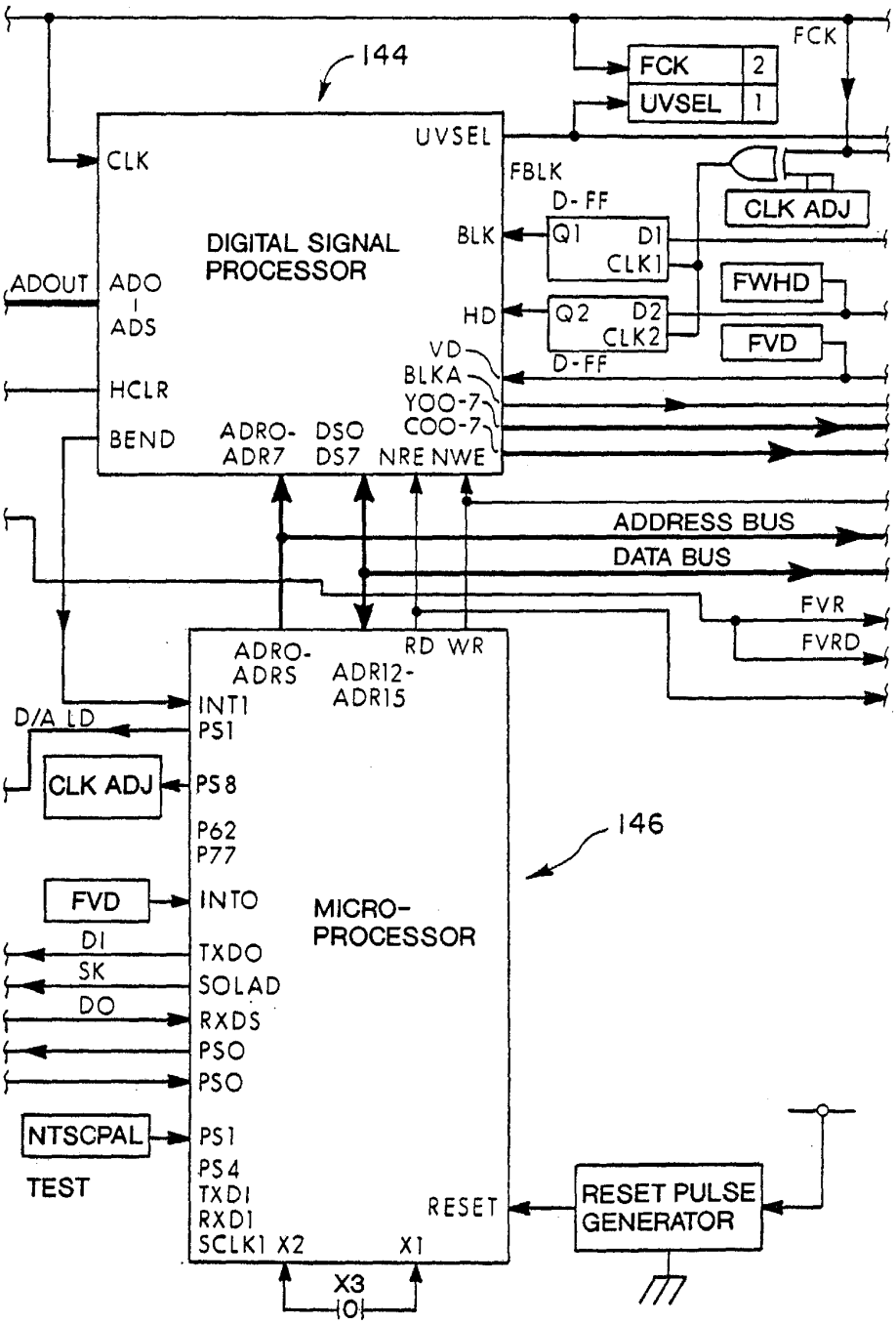
PBD
AMPQC
AGC CONT
08
TRAP
1.3V
3.0V
A/O OUT
Y OUT
AGC OUT
AMP IN
BUFFER
CP2
BUFFER
12-CH D/A CONVERTER
141
AQ 05
06
07
08
09
10
11
AQ03
AQ04
AQ01
AQ03
AQ012
FVR
FVRP
CA REF
3RS VADJ
SVADJ
LD
CLK
D1
EEPROM
DI
TR
DO
CS
ESSY
R
143

Fig. 8c


144
FCK
FCK 2
UVSEL 1
UVSEL
CLK
FBLK
D-FF
CLK ADJ
DIGITAL SIGNAL PROCESSOR
BLK
Q1 D1 CLK1
FWHD
ADOUT
ADO
ADS
HD
Q2 D2 CLK2
FVD
VD
BLKA
D-FF
HCLR
YOO-7
BEND
ADRO-ADR7
DSO DS7
COO-7
NRE NWE
ADDRESS BUS
DATA BUS
FVR
FVRD
ADRO-ADRS
ADR12-ADR15
RD WR
INT1
D/A LD
PS1
CLK ADJ
PS8
P62
P77
146
FVD
INTO
MICRO-PROCESSOR
DI
TXDO
SK
SOLAD
DO
RXDS
PSO
PSO
NTSCPAL
PS1
PS4
TEST
TXD1
RXD1
RESET
RESET PULSE GENERATOR
SCLK1 X2
X1
X3

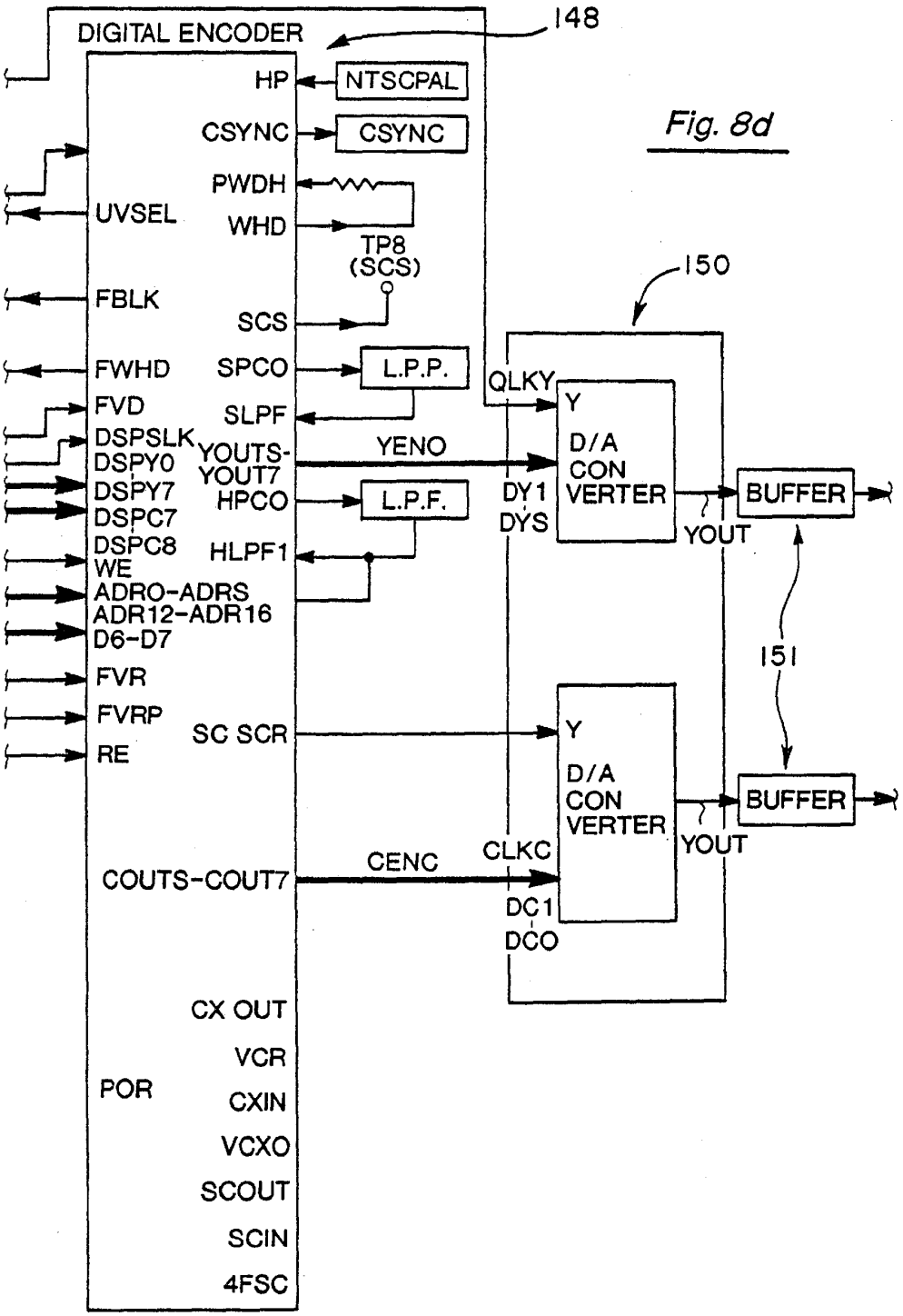

DIGITAL ENCODER
148
HP
NTSCPAL
CSYNC
CSYNC
PWDH
UVSEL
WHD
TP8
(SCS)
150
FBLK
SCS
FWHD
SPCO
L.P.P.
QLKY
Y
FVD
SLPF
DSPSLK
YOUTS-
YOUT7
YENO
D/A
CON
VERTER
BUFFER
DSPY0
DSPY7
DSPC7
HPCO
L.P.F.
DY1
DYS
YOUT
DSPC8
HLPF1
WE
ADR0-ADRS
ADR12-ADR16
D6-D7
151
FVR
FVRP
SC SCR
Y
RE
D/A
CON
VERTER
BUFFER
CLKC
CENC
YOUT
COUTS-COUT7
DC1
DCO
CX OUT
VCR
POR
CXIN
VCXO
SCOUT
SCIN
4FSC

Fig. 8d

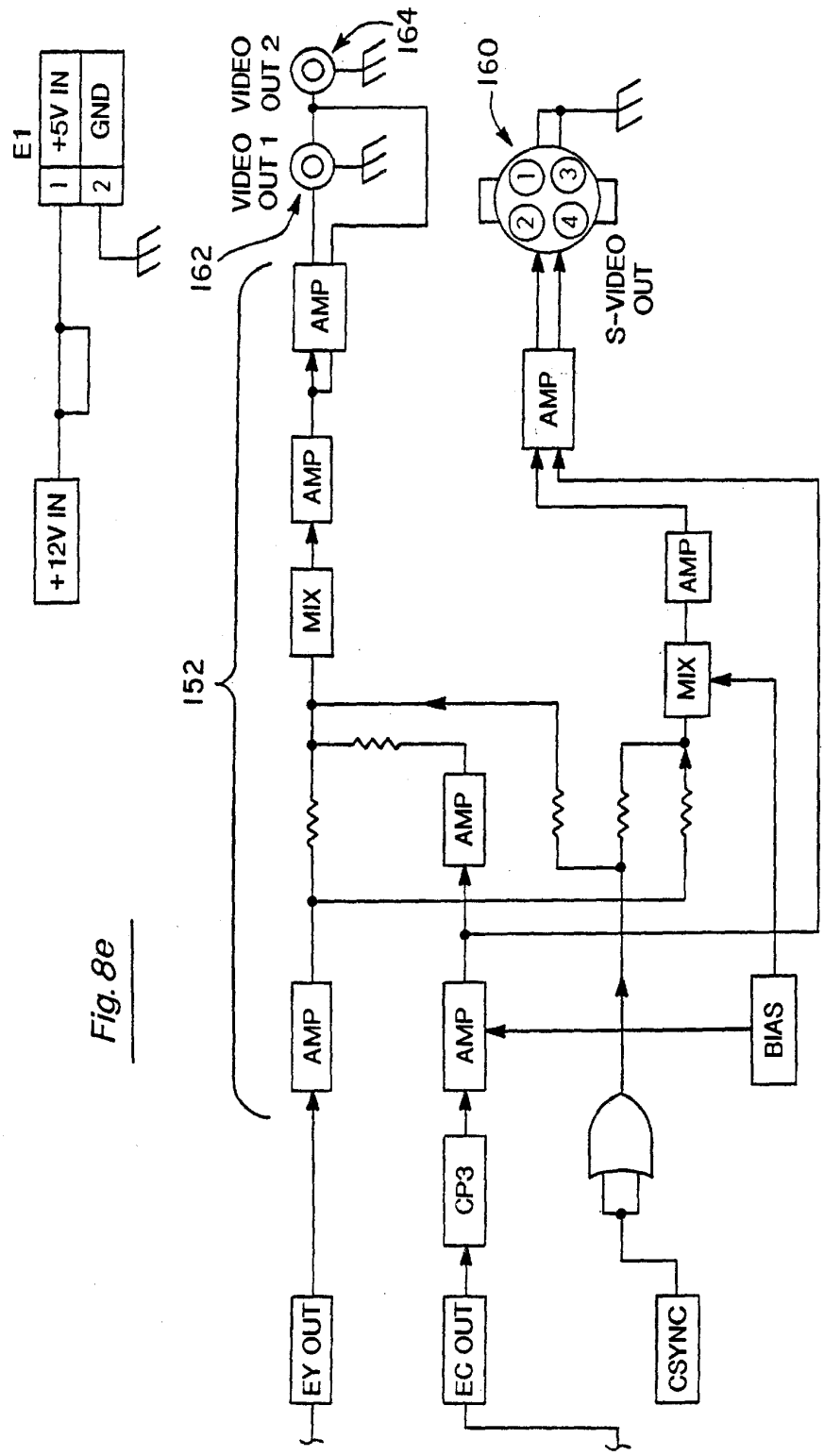

E1
+5V IN
GND
1
2
+12V IN
VIDEO OUT 2
VIDEO OUT 1
164
162
160
S-VIDEO OUT
AMP
MIX
152
BIAS
EY OUT
EC OUT
CP3
CSYNC

Fig. 8e

COMMUNICATION DEVICES INCORPORATING REDUCED AREA IMAGING DEVICES

This application is a continuation-in-part of U.S. Ser. No. 09/496,312, filed Feb. 1, 2000, and entitled "Reduced Area Imaging Devices", which is a continuation application of U.S. Ser. No. 09/175,685, filed Oct. 20, 1998 and entitled "Reduced Area Imaging Devices", now U.S. Pat. No. 6,043,839, which is a continuation-in-part of U.S. Ser. No. 08/944,322, filed Oct. 6, 1997 and entitled "Reduced Area Imaging Devices Incorporated Within Surgical Instruments", now U.S. Pat. No. 5,929,901.

TECHNICAL FIELD

This invention relates to solid state image sensors and associated electronics, and more particularly, to solid state image sensors which are configured to be of a minimum size and used within communication devices specifically including video telephones.

BACKGROUND ART

The three most common solid state image sensors include charged coupled devices (CCD), charge injection devices (CID) and photo diode arrays (PDA). In the mid-1980s, complementary metal oxide semiconductors (CMOS) were developed for industrial use. CMOS imaging devices offer improved functionality and simplified system interfacing. Furthermore, many CMOS imagers can be manufactured at a fraction of the cost of other solid state imaging technologies.

The CCD device is still the preferred type of imager used in scientific applications. Only recently have CMOS-type devices been improved such that the quality of imaging compares to that of CCD devices. However, there are enormous drawbacks with CCD devices. Two major drawbacks are that CCD device have immense power requirements, and the amount of processing circuitry required for a CCD imager always requires the use of a remote processing circuitry module which can process the image signal produced by the CCD imager. Also, because of the type of chip architecture used with CCD devices, on-chip processing is impossible. Therefore, even timing and control circuitry must be remoted from the CCD imager plane. Therefore, CCD technology is the antithesis of "camera on a chip" technology discussed below.

One particular advance in CMOS technology has been in the active pixel-type CMOS imagers which consist of randomly accessible pixels with an amplifier at each pixel site. One advantage of active pixel-type imagers is that the amplifier placement results in lower noise levels. Another major advantage is that these CMOS imagers can be mass produced on standard semiconductor production lines. One particularly notable advance in the area of CMOS imagers including active pixel-type arrays is the CMOS imager described in U.S. Pat. No. 5,471,515 to Fossum, et al. This CMOS imager can incorporate a number of other different electronic controls that are usually found on multiple circuit boards of much larger size. For example, timing circuits, and special functions such as zoom and anti-jitter controls can be placed on the same circuit board containing the CMOS pixel array without significantly increasing the overall size of the host circuit board. Furthermore, this particular CMOS imager requires 100 times less power than a CCD-type imager. In short, the CMOS imager disclosed in Fossum, et al. has enabled the development of a "camera on a chip."

Passive pixel-type CMOS imagers have also been improved so that they too can be used in an imaging device which qualifies as a "camera on a chip." In short, the major difference between passive and active CMOS pixel arrays is that a passive pixel-type imager does not perform signal amplification at each pixel site. One example of a manufacturer which has developed a passive pixel array with performance nearly equal to known active pixel devices and being compatible with the read out circuitry disclosed in the U.S. Pat. No. 5,471,515 is VLSI Vision, Ltd., 1190 Saratoga Avenue, Suite 180, San Jose, Calif. 95129. A further description of this passive pixel device may be found in co-pending application, Ser. No. 08/976,976, entitled "Reduced Area Imaging Devices Incorporated Within Surgical Instruments," now U.S. Pat. No. 5,986,693, and is hereby incorporated by reference.

In addition to the active pixel-type CMOS imager which is disclosed in U.S. Pat. No. 5,471,515, there have been developments in the industry for other solid state imagers which have resulted in the ability to have a "camera on a chip." For example, Suni Microsystems, Inc. of Mountain View, California, has developed a CCD/CMOS hybrid which combines the high quality image processing of CCDs with standard CMOS circuitry construction. In short, Suni Microsystems, Inc. has modified the standard CMOS and CCD manufacturing processes to create a hybrid process providing CCD components with their own substrate which is separate from the P well and N well substrates used by the CMOS components. Accordingly, the CCD and CMOS components of the hybrid may reside on different regions of the same chip or wafer. Additionally, this hybrid is able to run on a low power source (5 volts) which is normally not possible on standard CCD imagers which require 10 to 30 volt power supplies. A brief explanation of this CCD/CMOS hybrid can be found in the article entitled "Startup Suni Bets on Integrated Process" found in *Electronic News*, Jan. 20, 1997 issue. This reference is hereby incorporated by reference for purposes of explaining this particular type of imaging processor.

Another example of a recent development in solid state imaging is the development of a CMOS imaging sensor which is able to achieve analog to digital conversion on each of the pixels within the pixel array. This type of improved CMOS imager includes transistors at every pixel to provide digital instead of analog output that enable the delivery of decoders and sense amplifiers much like standard memory chips. With this new technology, it may, therefore, be possible to manufacture a true digital "camera on a chip." This CMOS imager has been developed by a Stanford University joint project and is headed by Professor Abbas el-Gamal.

A second approach to creating a CMOS-based digital imaging device includes the use of an over-sample converter at each pixel with a one bit comparator placed at the edge of the pixel array instead of performing all of the analog to digital functions on the pixel. This new design technology has been called MOSAD (multiplexed over sample analog to digital) conversion. The result of this new process is low power usage, along with the capability to achieve enhanced dynamic range, possibly up to 20 bits. This process has been developed by Amain Electronics of Simi Valley, California. A brief description of both of the processes developed by Stanford University and Amain Electronics can be found in an article entitled "A/D Conversion Revolution for CMOS Sensor?," September 1998 issue of *Advanced Imaging*. This reference is also hereby incorporated by reference for purposes of explaining these particular types of imaging processors.

Yet another example of a recent development with respect to solid state imaging is an imaging device developed by ShellCase, of Jerusalem, Israel. In an article entitled "A CSP Optoelectronic Package for Imaging and Light Detection Applications" (A. Badihi), ShellCase introduces a die-sized, ultrathin optoelectronic package which is completely packaged at the wafer level using semiconductor processing. In short, ShellCase provides a chip scale package (CSP) process for accepting digital image sensors which may be used, for example, in miniature cameras. The die-sized, ultrathin package is produced through a wafer level process which utilizes optically clear materials and completely encases the imager die. This packaging method, ideally suited for optoelectronic devices, results in superior optical performance and form factor not available by traditional image sensors. This reference is also incorporated by reference for purposes of explaining ShellCase's chip scale package process.

Yet another example of a recent development with respect to solid state imaging is shown in U.S. Pat. No. 6,020,581 entitled "Solid State CMOS Imager Using Silicon on Insulator or Bulk Silicon." This patent discloses an image sensor incorporating a plurality of detector cells arranged in an array wherein each detector cell as a MOSFET with a floating body and operable as a lateral bipolar transistor to amplify charge collected by the floating body. This reference overcomes problems of insufficient charge being collected in detector cells formed on silicon on insulator (SOI) substrates due to silicon thickness and will also work in bulk silicon embodiments.

The above-mentioned developments in solid state imaging technology have shown that "camera on a chip" devices will continue to be enhanced not only in terms of the quality of imaging which may be achieved, but also in the specific construction of the devices which may be manufactured by new breakthrough processes.

Although the "camera on a chip" concept is one which has great merit for application in many industrial areas, a need still exists for a reduced area imaging device which can be used in even the smallest type of industrial application. Recently, there have been developments with providing camera capabilities for wireless/cellular phones. Two-way still image video phones are making appearances on the market now. Additionally, there has been information regarding various worldwide manufacturers who are soon to come out with fully functional two-way video in combination with wireless/cellular phones. Because it is desirable to have a wireless/cellular phone of minimum size and weight, it is also desirable to have supporting imaging circuitry which is also of minimum size and weight. Accordingly, the invention described herein is ideal for use with upcoming video phone technology.

It is one object of this invention to provide a reduced area imaging device incorporated within a communication device which takes advantage of "camera on a chip" technology, but rearrange the circuitry in a selective stacked relationship so that there is a minimum profile presented when used within a communication device.

It is yet another object of this invention to provide imaging capability for a communication device wherein the camera used is of such small size that it can be attached to the communication device by a retractable cord which enables the imaging device to be used to image anything to which the camera is pointed at by the user without having to move the communication device away from the mouth when speaking.

In all applications, to include use of the imaging device of this invention with a communication device, "camera on a chip" technology can be improved with respect to reducing its profile area, and incorporating such a reduced area imaging device within a communication device such that minimal size and weight is added to the communication device, and further that the imaging device can be used to image selected targets by the user.

DISCLOSURE OF THE INVENTION

In accordance with the present invention, reduced area imaging devices are provided in combination with a communication device such as a wireless/cellular phone. The term "imaging device" as used herein describes the imaging elements and processing circuitry which is used to produce a video signal which may be accepted by both a standard video device such as a television or video monitor accompanying a personal computer, and a small LCD screen which is incorporated within the video phone. The term "image sensor" as used herein describes the components of a solid state imaging device which captures images and stores them within the structure of each of the pixels in the array of pixels found in the imaging device. As further discussed below, the timing and control circuits can be placed either on the same planar structure as the pixel array, in which case the image sensor can also be defined as an integrated circuit, or the timing and control circuitry can be placed remote from the pixel array. The terms "video signal" or "image signal" as used herein, and unless otherwise more specifically defined, refer to an image which at some point during its processing by the imaging device, is found in the form of electrons which have been placed in a specific format or domain. The term "processing circuitry" as used herein refers to the electronic components within the imaging device which receive the image signal from the image sensor and ultimately place the image signal in a usable format. The terms "timing and control circuits" or "timing and control circuitry" as used herein refer to the electronic components which control the release of the image signal from the pixel array.

In a first arrangement, the image sensor, with or without the timing and control circuitry, may be placed at the distal tip of a very small camera module which is attached by a cable or cord to the communication device, while the remaining processing circuitry may be placed within the housing of the communication device.

In a second arrangement, the image sensor and the processing circuitry may all be placed in a stacked arrangement of miniature circuit boards and positioned at the distal tip of the camera module. In this second arrangement, the pixel array of the image sensor may be placed by itself on its own circuit board while the timing and control circuitry and processing circuitry are placed on one or more other circuit boards, or the circuitry for timing and control may be placed with the pixel array on one circuit board, while the remaining processing circuitry can be placed on one or more of the other circuit boards.

In yet another alternative arrangement, the pixel array, timing and control circuits, and some of the processing circuitry can be placed near the distal end of the camera module with the remaining part of the processing circuitry being placed in the housing of the communication device.

For the arrangement or configuration of the imaging device which calls for the array of pixels and the timing and control circuitry to be placed on the same circuit board, only one conductor is required in order to transmit the image signal to the video processing circuitry when the timing and control circuits are incorporated onto other circuit boards, a

plurality of connections are required in order to connect the timing and control circuitry to the pixel array, and then the one conductor is also required to transmit the image signal to the video processing circuitry.

The invention disclosed herein can also be considered an improvement to a cellular/wireless phone wherein the improvement comprises a video system. The video system would include the video monitor attached to the phone, the camera module, the imaging device within the camera module, as well as supporting video processing circuitry for the imaging device. In yet another aspect, the invention disclosed herein can also be considered an improvement to a video telephone wherein the improvement comprises a novel imaging device, preferably of CMOS construction. For this improvement comprising the imaging device, the imaging device includes the array of pixels, and the supporting video processing circuitry for providing a video ready signal.

The video ready signal produced by the video processing circuitry may be of differing video formats for viewing on different types of video devices. For example, the video ready signal may be a NTSC/PAL compatible video signal for viewing on a remote video device such as a TV; the video signal may be a YUV 4:2:2 signal for viewing on a video monitor attached to the phone; and/or the video signal may be VGA compatible for viewing on a personal computer. Accordingly, the invention disclosed herein has utility with respect to an overall combination of elements, as well as various sub-combination of elements.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an enlarged fragmentary partially exploded perspective view of the distal end of the camera module which is used in conjunction with the communication device, specifically illustrating the arrangement of the image sensor with respect to the other elements of the camera module;

FIG. **1***a* is an enlarged exploded perspective view illustrating another configuration of the image sensor wherein video processing circuitry is placed behind and in longitudinal alignment with the image sensor;

FIG. **2** is a perspective view of the communication device incorporating the reduced area imaging device of this invention, and further illustrating the video monitor in operation, along with the camera module pulled out in the extended position;

FIG. **3** illustrates the communication device of FIG. **2** wherein the camera module is in the retracted position, along with the video monitor in the folded or retracted position;

FIG. **4** is another perspective view of the communication device of this invention illustrating an alternative arrangement for placement of the video monitor within a flip panel;

FIG. **5** is a perspective view of the communication device of FIG. **4** illustrating the alternative arrangement of the video monitor with the video monitor stored within the folded flip panel;

FIG. **6** is an overall schematic diagram of the functional electronic components which make up both the communication device, and the reduced area imaging device;

FIG. **7** is a more detailed schematic diagram of the functional electronic components which make up the imaging device;

FIG. **7***a* is an enlarged schematic diagram of a circuit board/planar structure which may include the array of pixels and the timing and control circuitry;

FIG. **7***b* is an enlarged schematic diagram of a video processing board/planar structure having placed thereon the processing circuitry which processes the pre-video signal generated by the array of pixels and which converts the pre-video signal to a post-video signal which may be accepted by an NTSC/PAL compatible video device; and

FIGS. **8***a*–**8***e* are schematic diagrams that illustrate an example of specific circuitry which may be used to make the video processing circuitry of the imaging device.

BEST MODE FOR CARRYING OUT THE INVENTION

In accordance with the invention, as shown in FIG. **1**, a camera module **10** is provided which incorporates a reduced area imaging device **11**. As further discussed below, the elements of the imaging device **11** may all be found near one location, or the elements may be separated from one another and interconnected by the appropriate wired connections. The array of pixels making up the image sensor captures images and stores them in the form of electrical energy by conversion of light photons to electrons. This conversion takes place by the photo diodes in each pixel which communicate with one or more capacitors which store the electrons. Specifically, the camera module **10** includes an outer tube/sheath **14** which houses the components of the imaging device. The camera module is shown as being cylindrical in shape having a window **16** sealed at the distal end of the camera module. A retractable cable **12** extends from the proximal end of the camera module **10**. A shielded cable **21** is used to house the conductors which communicate with the imaging device **11**. The shielded cable **21** is then housed within the retractable cable **12**. A lens group **18** is positioned at the distal end of the camera module to enable an image to be appropriately conditioned prior to the image impinging upon the imaging device **11**. Also shown is a focusing ring **20** which enables the lens group **18** to be displaced distally or proximally to best focus an image on the imaging device **11**.

Now referring to FIGS. **2**–**5**, a video phone **22** is shown which incorporates the camera module **10**. In basic terms, the video phone is simply a standard wireless/cellular phone which has added thereto the ability to send and receive video signals which may both be viewed on video monitor **30**. Beginning first with a description of the basic components of the video phone, it includes a phone housing **24** which holds the components of the video phone. Cable **12** is housed within the housing **24** when in the retracted position. A spring biased spool (not shown) or some other known retracting device is mounted within the housing **24** enabling the cable **12** to be extended or retracted. When the cable is retracted, the camera module **10** can be stored within cavity or opening **25** at the base of housing **24**. This cavity or opening **25** can substantially conform to the size and shape of the camera module **10**. The camera module **10** is illustrated as being elongate and cylindrical, minimizing its size and profile, and enhancing its ability to be stored within opening **25**. As shown in FIG. **3**, when the camera module **10** is stored, it does not increase the overall size of the video telephone **22**, and does not protrude away from the phone housing **24**, thus making the camera module **10** a component which truly integrates with the housing **24** of the video phone **22**. The cable **12** is of a selected length which allows the user to point the camera module **10** toward a targeted object to taking video. A keypad **26** is provided enabling a user to dial the phone, or achieve other well-known telephone functions. An audio receiving assembly **27** in the conventional manner is provided which allows the user to

listen to incoming audio. This assembly may later be referred to simply as a speaker. An orifice or hole **28** is provided which communicates with a microphone (discussed below) for transmitting audio signals. The phone display **29** displays the various functions of the phone as controlled by a user. The display **29** in most wireless/cellular phones is a liquid crystal display. The video monitor **30** attaches to the housing **24** as by linkage **31**. As shown, two pieces of linkage are provided, along with three ball/socket type joints **32** which enable the video monitor to be articulated to the desired position with respect to the housing **24**. An internal video cable **33** having a plurality of conductors (not shown) extends through the linkage **31** and the ball and socket joints **32** for providing the video signals which are displayed on the video monitor **30**. The video monitor **30** may be a liquid crystal display (LCD) type, or any other well-known display device of high resolution which has low power requirements, and has minimum size requirements as well. An example of a manufacture of such a miniature LCD monitor includes DISPLAYTECH of Longmont, Colo. DISPLAYTECH manufactures a miniature reflective display that consists of ferroelectric liquid crystal (FLC) applied to a CMOS integrated circuit. The reflective display is a VGA display panel having low voltage digital operation, low power requirements, and full color operation. One of their specific products includes the LightCaster™ VGA Display Panel, Model LDP-0307-MV1. This is but one example of an LCD monitor which is available and usable within the invention herein described. As further discussed below, a video select switch **34** is mounted on the housing **24** which enables a user to select viewing of either incoming video signals, or to view the outgoing video signals which are those images taken by the camera module **10**. A conventional antenna **35** is provided to enhance reception and transmission capabilities of the video phone.

FIGS. **4** and **5** illustrate a modification of the video phone of FIGS. **2** and **3**. Specifically, FIGS. **4** and **5** illustrate an alternative way in which to attach the video monitor **30** to the video phone **22**. As shown, FIGS. **4** and **5** illustrate a flip panel **36** which attaches to the base of the housing **24** as by hinge **39**. The video monitor itself is then mounted to the flip panel **36** as by hinge **37**. Video signals are transmitted to the video monitor **30** of FIGS. **4** and **5** by the conductors housed in video cable **33**. As shown, video cable **33** is routed through the flip panel **36**. The video monitor **30** of FIGS. **4** and **5** can be placed in the desired position by rotating the flip panel **36** about hinge **39**, and then rotating the video monitor **30** about hinge **37**.

Referring back to FIGS. **1** and **1***a*, the imaging device **11** includes an image sensor **40**. FIG. **1** illustrates that the image sensor **40** can be a planar and square shaped member, or alternatively, planar and circular shaped to better fit within outer tube **14**. In the configuration of the imaging device in FIGS. **1** and **1***a*, there are only three conductors which are necessary for providing power to the image sensor **40**, and for transmitting an image from the image sensor **40** back to the processing circuitry found within the phone housing **24**. Specifically, there is a power conductor **44**, a grounding conductor **46**, and an image signal conductor **48**, each of which are hardwired to the image sensor **40**. Thus, shielded cable **21** may simply be a three conductor, 50 ohm type cable.

Image sensor **40** can be as small as 1 mm in its largest dimension. However, a more preferable size for most video phone applications would be between 4 mm to 8 mm in the image sensor's largest dimension (height or width). The image signal transmitted from the image sensor **40** through conductor **48** is also herein referred to as a pre-video signal. Once the pre-video signal has been transmitted from image sensor **40** by means of conductor **48**, it is received by video processing board **50**, as shown in FIG. **6**. Video processing board **50** then carries out all the necessary conditioning of the pre-video signal and places it in a form, also referred to herein as a video ready signal, so that it may be viewed directly on a remote video device such as a television or standard computer video monitor. In order for the pre-video signal to be viewed on the monitor **30**, the pre-video signal is further conditioned by a digital signal processor **72**, as further discussed below. The video signal produced by the video processing board **50** which is viewable by an NTSC/PAL compatible video device (such as a television) can be further defined as a post-video signal.

FIG. **1** illustrates an arrangement wherein the image sensor **40** is placed by itself adjacent the distal end of the camera module **10**. Alternatively, some or all of the video processing circuitry may be placed in adjacent circuit boards directly behind the image sensor **40**. Accordingly, **1***a* illustrates video processor board **50** aligned directly behind the image sensor **40**. A plurality of pin connectors **52** can be used to interconnect image sensor **40** to video processor board **50**. Depending upon the specific configuration of image sensor **40**, pin connectors **52** may be provided for structural support and/or to provide a means by which image signals are transmitted between image sensor **40** and board **50**. Additionally, digital signal processor **72** could also be placed behind image sensor **40** and behind video processing board **50**. Accordingly, the image sensor, and all supporting video processing circuitry could be placed at the distal end of the camera module **10**. However, because of the ample space within housing **24**, it may be preferable to place at least some of the video processing circuitry within housing **24**. In the case of FIG. **1***a*, the conductor **49** represents the conductor which may carry the post-video signal for direct connection with a remote video device **60** such as a television or computer monitor. As also discussed further below, placement of the digital signal processor **72** at the distal tip of the camera module behind the video processing board **50** would also enable yet another conductor (not shown) to connect directly to the video monitor **30** for transmitting a video ready signal to the video monitor **30**.

Referring back to FIG. **1**, the area which is occupied by image sensor **40** may be defined as the profile area of the imaging device and which determines its critical dimensions. If it is desired to place video processing circuitry adjacent the image sensor **40** at the distal end of the camera module **10**, such circuitry must be able to be placed on one or more circuit boards which are longitudinally aligned with image sensor **40** along longitudinal axis XX. If it is not important to limit the size of the profile area, then any circuitry placed behind image sensor **40** can be aligned in an offset manner, or may simply be larger than the profile area of image sensor **40**. In the configuration shown in FIG. **1***a*, it is desirable that elements **40** and **50** be approximately the same size so that they may uniformly fit within the distal end of outer tube **14**.

Now referring to FIG. **6**, a further explanation is provided of the basic electronic components of the video phone **22** which combines circuitry and functionality of a standard mobile/wireless phone and a video system. One example of a patent disclosing basic mobile phone technology including a discussion of basic phone circuitry is U.S. Pat. No. 6,018,670. This patent is hereby incorporated by reference in its entirety for purposes of disclosing standard or basic mobile phone technology and supporting circuitry. As

shown in FIG. **6**, a conventional cellular phone battery **62** is provided which communicates with power supply board **64**. Power supply board **64** conditions various power outputs to the components of the device, to include power to the video components. In the preferred imaging device of this invention, the power to the imaging device may simply be direct current of between about 1.5 to 12 volts, depending upon the power requirements of the imaging device. A camera on/off switch **66** must be set to the "on" position in order to activate the camera module **10**. The video processor board **50** then transfers power to supplies the camera module **10**, and also receives the analog pre-video signal back from the camera module, as further discussed below. After processing of the pre-video signal at the video processor board **50**, the video signal is video ready, meaning that it may then be directly viewed on a remote compatible video device **60**, such as a television or computer monitor. A video port **54** can be provided on the housing **24** enabling a user to take a standard video jack and interconnect the video phone with the video port of the remote video device. The video format for such remote video devices includes NTSC/PAL and VGA; thus, the video signal processed by video processor board **50** creates the video ready signals for use with these remote video devices. For purposes of viewing images on the monitor **30**, the pre-video signal is further processed into a digital format within video processor board **50**, preferably an 8 bit composite video signal format that is commonly referred to as "YUV 4:2:2." This video format easily lends itself to video compression. This 8 bit digital video signal is then sent to the digital signal processor **72** which performs two functions relevant to the video signal. The digital signal processor **72** further converts the signal into a format that is compatible with the driver circuitry of the video monitor **30**. Secondly, the digital signal processor **72** compresses the YUV signal using a common video compression format, preferably JPEG. The JPEG encoded video signal is then mixed with the audio signal created by microphone **78** and amplifier **74**, and the resulting high frequency carrier signal may then be passed onto the transceiver/amplifier section **70** for transmission. The transceiver/amplifier section also modulates the carrier signal prior to transmission. Depending upon the position of video switch **34**, the video signal from digital signal processor **72** is either sent to the monitor **30**, or is sent to the transceiver/amplifier section **70** for transmission. As also shown, the antenna **35** is used for enhancement of reception and transmission of transmitted and received carrier signals.

The transceiver/amplifier section **70** also serves as a receiver which receives an incoming carrier signal. This incoming signal is then demodulated within section **70**, the video and audio components of the incoming signal are separated, and then these separated signals are then sent to the digital signal processor **72** which performs video decompression. Then, the decompressed video signal is sent to the monitor **30** for viewing (if the video switch **34** is placed in that selected mode). The decompressed audio signal is sent to the amplifier **74**, and then to the speaker **76**. The video switch **34** may simply be a momentary, spring loaded, push button-type switch. When the video switch **34** is not depressed, incoming video, which is received via the handset antenna **35**, is processed as discussed above in the transceiver/amplifier section **70** and digital signal processor **72**, and then sent to the monitor **30**. When the video switch **34** is depressed and held, the video signal produced from the camera module **10** is processed as discussed above, and ultimately sent to the monitor **30**. An operator can cycle the switch **34** between the two positions in order to selectively choose whether to view incoming or outgoing video.

To summarize the operation of the video telephone, a user wishing to contact another party would dial the telephone in the conventional manner. Assuming the party called has video telephone capability, the user could view the images transmitted from the other party by not depressing the video switch **34**. If the user desires to transmit video images to the other party, the user would grasp the camera module **10**, and extend the cord **12** of the camera module by pulling it away from the video telephone, and then point the camera module at the object/person targeted. The user then depresses the video switch **34** which transmits to the other party the images captured by the camera module **10**. Also, the video monitor **30** will display the images captured by the camera module **10** by depressing the video switch **34**. Because the camera module is tethered to the video telephone by retractable cable **12**, the user can continue a conversation with the other party without having to physically remove the video telephone away from the user's mouth when simultaneously taking video by the camera module. Because of the extremely small size of the camera module **10**, it is easily housed within the housing **24** when not in use.

FIG. **7** is a schematic diagram illustrating one way in which the imaging device **11** may be constructed. As illustrated, the image sensor **40** may include the timing and control circuits on the same planar structure.

Power is supplied to image sensor **40** by power supply board **64**. The connection between image sensor **40** and board **64** may simply be a cable having two conductors therein, one for ground and another for transmitting the desired voltage. These are illustrated as conductors **44** and **46**. The output from image sensor **40** in the form of the pre-video signal is input to video processor board **50** by means of the conductor **48**. In the configuration of FIG. **4**, conductor **48** may simply be a 50 ohm conductor. Power and ground also are supplied to video processing board **50** by conductors **44** and **46** from power supply board **52**. The output signal from the video processor board **50** is in the form of the post-video signal and which may be carried by conductor **49** which can also be a 50 ohm conductor.

Although FIG. **7** illustrates the image sensor and the timing and control circuits being placed on the same circuit board or planar structure, it is possible to separate the timing and control circuits from the pixel array and place the timing and control circuits onto video processing board **50**.

The advantage in placing the timing and control circuits on the same planar structure as the image sensor is that only three connections are required between image sensor **40** and the rest of the imaging device, namely, conductors **44**, **46** and **48**. Additionally, placing the timing and control circuits on the same planar structure with the pixel array results in the pre-video signal having less noise. Furthermore, the addition of the timing and control circuits to the same planar structure carrying the image sensor only adds a negligible amount of size to one dimension of the planar structure. If the pixel array is to be the only element on the planar structure, then additional connections must be made between the planar structure and the video processing board **50** in order to transmit the clock signals and other control signals to the pixel array. For example, a ribbon-type cable (not shown) or a plurality of 50 ohm coaxial cables (not shown) must be used in order to control the downloading of information from the pixel array. Each of these additional connections would be hard wired between the boards.

FIG. **7***a* is a more detailed schematic diagram of image sensor **40** which contains an array of pixels **90** and the timing and control circuits **92**. One example of a pixel array

90 which can be used within the invention is similar to that which is disclosed in U.S. Pat. No. 5,471,515 to Fossum, et al., said patent being incorporated by reference herein. More specifically, FIG. 3 of Fossum, et al. illustrates the circuitry which makes up each pixel in the array of pixels 90. The array of pixels 90 as described in Fossum, et al. is an active pixel group with intra-pixel charged transfer. The image sensor made by the array of pixels is formed as a monolithic complementary metal oxide semiconductor (CMOS) integrated circuit which may be manufactured in an industry standard complementary metal oxide semiconductor process. The integrated circuit includes a focal plane array of pixel cells, each one of the cells including a photo gate overlying the substrate for accumulating the photo generated charges. In broader terms, as well understood by those skilled in the art, an image impinges upon the array of pixels, the image being in the form of photons which strike the photo diodes in the array of pixels. The photo diodes or photo detectors convert the photons into electrical energy or electrons which are stored in capacitors found in each pixel circuit. Each pixel circuit has its own amplifier which is controlled by the timing and control circuitry discussed below. The information or electrons stored in the capacitors is unloaded in the desired sequence and at a desired frequency, and then sent to the video processing board 50 for further processing.

Although the active pixel array disclosed in U.S. Pat. No. 5,471,515 is mentioned herein, it will be understood that the hybrid CCD/CMOS described above, or any other solid state imaging device may be used wherein timing and control circuits can be placed either on the same circuit board or planar structure with the pixel array, or may be separated and placed remotely. Furthermore, it will be clearly understood that the invention claimed herein is not specifically limited to an image sensor as disclosed in the U.S. Pat. No. 5,471,515, but encompasses any image sensor which may be configured for use in conjunction with the other processing circuitry which makes up the imaging device of this invention.

To summarize the different options available in terms of arrangement of the components of the imaging device 11, the array of pixels 90 of the image sensor 40 may be placed alone on a first plane, or the timing and control circuitry 92 may be placed with the array of pixels 90 on the first plane. If the timing and control circuitry 92 is not placed with the array of pixels 90 on the first plane, the timing and control circuitry 92 may be placed by itself on a second plane, or the timing and control circuitry 92 may be placed on a second plane with some or all of the processing circuitry from video processing board 50. The video processing board 50 itself may be placed on one or more planes on corresponding circuit boards containing video processing circuitry. FIG. 1*a* illustrates a single video processor board 50 located directly behind image sensor 40; however, it shall be understood that additional circuit boards containing additional circuitry may be placed behind the image sensor 40 and behind the video processing board 50. Some or all of the video processing circuitry may be placed within the camera module 10 near the distal end thereof adjacent the image sensor 40. Video processing circuitry which is not placed within the distal end of the camera module 10 may be placed within the housing 24 of the communication device. If video processing circuitry is placed near the distal end of the camera module 10, it is preferable to arrange the video processing circuitry in a stacked relationship behind the image sensor 40. Additionally, it is preferable to place the processing circuitry in a parallel arrangement with respect to image sensor 40 and to center such video processing circuitry along axis X—X in order to minimize the size of camera module 10.

The timing and control circuits 92 are used to control the release of the image information or image signal stored in the pixel array. In the image sensor of Fossum, et al., the pixels are arranged in a plurality of rows and columns. The image information from each of the pixels is first consolidated in a row by row fashion, and is then downloaded from one or more columns which contain the consolidated information from the rows. As shown in FIG. 7*a*, the control of information consolidated from the rows is achieved by latches 94, counter 96, and decoder 98. The operation of the latches, counter and decoder is similar to the operation of similar control circuitry found in other imaging devices. That is, a latch is a means of controlling the flow of electrons from each individual addressed pixel in the array of pixels. When a latch 94 is enabled, it will allow the transfer of electrons to the decoder 98. The counter 96 is programmed to count a discrete amount of information based upon a clock input from the timing and control circuits 92. When the counter 96 has reached its set point or overflows, the image information is allowed to pass through the latches 94 and be sent to the decoder 98 which places the consolidated information in a serial format. Once the decoder 98 has decoded the information and placed it in the serial format, then the row driver 100 accounts for the serial information from each row and enables each row to be downloaded by the column or columns. In short, the latches 94 will initially allow the information stored in each pixel to be accessed. The counter 96 then controls the amount of information flow based upon a desired time sequence. Once the counter has reached its set point, the decoder 98 then knows to take the information and place it in the serial format. The whole process is repeated, based upon the timing sequence that is programmed. When the row driver 100 has accounted for each of the rows, the row driver reads out each of the rows at the desired video rate.

The information released from the column or columns is also controlled by a series of latches 102, a counter 104 and a decoder 106. As with the information from the rows, the column information is also placed in a serial format which may then be sent to the video processing board 50. This serial format of column information is the pre-video signal carried by conductor 48. The column signal conditioner 108 places the column serial information in a manageable format in the form of desired voltage levels. In other words, the column signal conditioner 108 only accepts desired voltages from the downloaded column(s).

The clock input to the timing and control circuits 92 may simply be a quartz crystal timer. This clock input is divided into many other frequencies for use by the various counters. The run input to the timing and control circuit 92 may simply be an on/off control. The default input can allow one to input the pre-video signal to a video processor board which may run at a frequency of other than 30 hertz. The data input controls functions such as zoom. At least for a CMOS type active pixel array which can be accessed in a random manner, features such as zoom are easily manipulated by addressing only those pixels which locate a desired area of interest by the user.

A further discussion of the timing and control circuitry which may be used in conjunction with an active pixel array is disclosed in U.S. Pat. No. 5,471,515 and is also described in an article entitled "Active Pixel Image Sensor Integrated With Readout Circuits" appearing in *NASA Tech Briefs*, October 1996, pp. 38 and 39. This particular article is also incorporated by reference.

Once image sensor **40** has created the pre-video signal, it is sent to the video processing board **50** for further processing. At board **50**, as shown in FIG. **7***b*, the pre-video signal is passed through a series of filters. One common filter arrangement may include two low pass filters **114** and **116**, and a band pass filter **112**. The band pass filter only passes low frequency components of the signal. Once these low frequency components pass, they are then sent to detector **120** and white balance circuit **124**, the white balance circuit distinguishing between the colors of red and blue. The white balance circuit helps the imaging device set its normal, which is white. The portion of the signal passing through low pass filter **114** then travels through gain control **118** which reduces the magnitude or amplitude of this portion to a manageable level. The output from gain control **118** is then fed back to the white balance circuit **124**. The portion of the signal traveling through filter **116** is placed through the processor **122**. In the processor **122**, the portion of the signal carrying the luminance or non-chroma is separated and sent to the Y chroma mixer **132**. Any chroma portion of the signal is held in processor **122**.

Referring to the output of the white balance circuit **124**, this chroma portion of the signal is sent to a delay line **126** where the signal is then further reduced by switch **128**. The output of switch **128** is sent through a balanced modulator **130** and also to the Y chroma mixer **132** where the processed chroma portion of the signal is mixed with the processed non-chroma portion. Finally, the output from the Y chroma mixer **132** is sent to the NTSC/PAL encoder **134**, commonly known in the art as a "composite" encoder. The composite frequencies are added to the signal leaving the Y chroma mixer **132** in encoder **134** to produce the post-video signal which may be accepted by a television. Additionally, the signal from Y chroma mixer **132** is sent to the digital signal processor **72** so that images can be viewed on monitor **30**.

In addition to the functions described above that are achieved by the digital signal processor **72**, the processor **72** can also provide additional digital enhancements. Specifically, digital enhancement can sharpen or otherwise clarify the edges of an image viewed on a video screen which might normally be somewhat distorted. Additionally, selected background or foreground images may be removed thus only leaving the desired group of images.

In addition to digital enhancement, the digital signal processor **72** can include other circuitry which may further condition the signal received from board **50** so that it may be viewed in a desired format other than NTSC/PAL. One common encoder which can be used would be an RGB encoder. An RGB encoder separates the signal into the three primary colors (red, green and blue). A SVHS encoder (super video home system) encoder could also be added to processor **72**. This type of encoder splits or separates the luminance portion of the signal and the chroma portion of the signal. Some observers believe that a more clear signal is input to the video device by such a separation, which in turn results in a more clear video image viewed on the video device. Another example of an encoder which could be added to processor **72** includes a VGA compatible encoder, which enables the video signal to be viewed on a standard VGA monitor which is common to many computer monitors.

One difference between the arrangement of image sensor **40** and the outputs found in FIG. **3** of the Fossum, et al. patent is that in lieu of providing two analog outputs [namely, VS out (signal) and VR out (reset)], the reset function takes place in the timing and control circuitry **92**. Accordingly, the pre-video signal only requires one conductor **48**.

FIGS. **8***a*–**8***e* illustrate in more detail one example of circuitry which may be used in the video processing board **50** in order to produce a post-video signal which may be directly accepted by a NTSC/PAL compatible video device such as a television. The circuitry disclosed in FIGS. **8***a*–**8***e* is very similar to circuitry which is found in a miniature quarter-inch Panasonic camera, Model KS-162. It will be understood by those skilled in the art that the particular arrangement of elements found in FIGS. **8***a*–**8***e* are only exemplary of the type of video processing circuitry which may be incorporated in order to take the pre-video signal and condition it to be received by a desired video device.

As shown in FIG. **8***a,* 5 volt power is provided along with a ground by conductors **44** and **46** to board **50**. The pre-video signal carried by conductor **48** is buffered at buffer **137** and then is transferred to amplifying group **138**. Amplifying group **138** amplifies the signal to a usable level as well as achieving impedance matching for the remaining circuitry.

The next major element is the automatic gain control **140** shown in FIG. **8***b*. Automatic gain control **140** automatically controls the signal from amplifying group **138** to an acceptable level and also adds other characteristics to the signal as discussed below. More specifically, automatic gain control **140** conditions the signal based upon inputs from a **12** channel digital to analog converter **141**. Converter **141** retrieves stored information from EEPROM (electrically erasable programmable read only memory) **143**. EEPROM **143** is a non-volatile memory element which may store user information, for example, settings for color, tint, balance and the like. Thus, automatic gain control **140** changes the texture or visual characteristics based upon user inputs. The keypad **26**, in addition to the conventional buttons used to control telephone communications, could also include buttons for controlling the image viewed on monitor **30** such as a gain control **140**. The signal leaving the automatic gain control **140** is an analog signal until being converted by analog to digital converter **142**.

Digital signal processor **144** of FIG. **8***c* further processes the converted signal into a serial type digital signal. One function of the microprocessor **146** is to control the manner in which digital signal processor **144** sorts the digital signals emanating from converter **142**. Microprocessor **146** also controls analog to digital converter **142** in terms of when it is activated, when it accepts data, when to release data, and the rate at which data should be released. Microprocessor **146** may also control other functions of the imaging device such as white balance. The microprocessor **146** may selectively receive the information stored in the EEPROM **143** and carry out its various commands to further control the other elements within the circuitry.

After the signal is processed by digital signal processor **144**, the signal is sent to digital encoder **148** illustrated in FIG. **8***d*. Some of the more important functions of digital encoder **148** are to encode the digital signal with synchronization, modulated chroma, blanking, horizontal drive, and the other components necessary so that the signal may be placed in a condition for reception by a video device such as a television monitor. As also illustrated in FIG. **8***d*, once the signal has passed through digital encoder **148**, the signal is reconverted into an analog signal through digital to analog converter **150**.

This reconverted analog signal is then buffered at buffers **151** and then sent to amplifier group **152** of FIG. **8***e* which amplifies the signal so that it is readily accepted by a desired video device. Specifically, as shown in FIG. **8***e*, one SVHS outlet is provided at **160**, and two composite or NTSC outlets are provided at **162** and **164**, respectively.

From the foregoing, it is apparent that an entire imaging device may be incorporated within the distal tip of the camera module, or may have some elements of the imaging device being placed in the housing of the communication device. Based upon the type of image sensor used, the profile area of the imaging device may be made small enough to be placed into a camera module which has a very small diameter.

This invention has been described in detail with reference to particular embodiments thereof, but it will be understood that various other modifications can be effected within the spirit and scope of this invention.

What is claimed is:

1. In a wireless telephone for conducting wireless telephonic communications, the improvement comprising:

a video system integral with said telephone for receiving and transmitting video images, and for viewing said video images, said video system comprising;

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of CMOS pixels for timing and control of said array of CMOS pixels, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically coupled to said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;

a video monitor attached to said wireless phone for viewing said video images, said video monitor communicating with said first circuit board, and displaying video images processed by said first circuit board.

2. A device, as claimed in claim **1**, wherein:

said first circuit board is placed adjacent said image sensor within said camera module.

3. A device, as claimed in claim **1**, wherein:

said first circuit board is remote from said image sensor and placed within a housing of said telephone.

4. A device, as claimed in claim **1**, wherein:

said image sensor defines a profile area in said first plane, and said first circuit board is positioned in longitudinal alignment with said image sensor such that said first circuit board does not extend substantially beyond said profile area.

5. A device, as claimed in claim **1**, further including:

a second circuit board electrically coupled with said first circuit board and said image sensor for further processing said pre-video signal, said second board being placed adjacent said first circuit board within said camera module.

6. A device, as claimed in claim **1**, wherein:

said first and second planes are offset from and substantially parallel to one another.

7. A device, as claimed in claim **5**, wherein:

said second circuit board lies in a third plane which is offset from and extends substantially parallel to said first and second planes.

8. A device, as claimed in claim **5**, wherein:

said second circuit board includes means for digital signal processing enabling the pre-video signal conditioned by said first circuit board to be viewed by said video monitor.

9. A device, as claimed in claim **1**, wherein:

said first circuit board converts said pre-video signal to a post-video signal for direct reception by a remote video device, said post-video signal being of a format selected from the group consisting of a NTSC/PAL video signal and a VGA video signal.

10. A device, as claimed in claim **1**, wherein:

said array of CMOS pixels includes an array of passive CMOS pixels, wherein individual passive CMOS pixels of said array of passive CMOS pixels each include a photo diode for producing photoelectrically generated signals, and an access transistor communicating with said photo diode to control the release of photoelectrically generated signals.

11. A device, as claimed in claim **1**, wherein:

individual pixels within said array of CMOS pixels each include an amplifier.

12. A device, as claimed in claim **1**, further including:

a retractable cable interconnecting said camera module to said wireless phone, said retractable cable enabling said camera module to be pulled away from said wireless telephone for selective taking of images by said camera module, and allowing said camera module to be stored within said wireless telephone by retracting said cable and securing said camera module within said wireless telephone.

13. A device, as claimed in claim **1**, wherein:

said wireless phone further includes a flip panel hingedly connected thereto, and wherein said video monitor is hingedly connected to said flip panel.

14. A device as claimed in claim **1**, further including:

adjustable linkage interconnecting said video monitor to said wireless phone.

15. A device, as claimed in claim **1**, further including:

a remote video device electrically coupled to said video system for further viewing said video images.

16. A device, as claimed in claim **15**, wherein:

said remote video device is selected from the group consisting of a television and a computer monitor.

17. In a video telephone for receiving and transmitting telephone communications to include video signals transmitted by the user of the phone, and video signals received from the party to whom a call was made, the video telephone including a housing, and a video monitor for viewing the video signals the improvement comprising:

a camera module for taking video images, said camera module communicating with circuitry within said video telephone enabling viewing on said video telephone and enabling video signals to be viewing on said video telephone and enabling video signals to be transmitted from said camera module for viewing by said party, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of said CMOS pixels for timing and control of said array of CMOS pixels, said image sensor producing a pre-video signal, a first circuit board electrically connected to said image sensor and residing on a second plane, said first circuit board including circuitry means for converting said pre-video signal to a desired video format.

18. A device, as claimed in claim **17**, wherein:

said first circuit board is placed adjacent said image sensor within said camera module.

19. A device, as claimed in claim 17, wherein:
said first circuit board is placed within said housing of said telephone.
20. A device, as claimed in claim 17, wherein:
said image sensor defines a profile area in said first plane, and said first circuit board is positioned in longitudinal alignment with said image sensor such that said first circuit board does not extend substantially beyond said profile area.
21. A device, as claimed in claim 17, further including:
a second circuit board electrically coupled with said first circuit board and said image sensor for further processing said pre-video signal, said second board being placed adjacent said first circuit board within said camera module.
22. A device, as claimed in claim 17, wherein:
said first and second planes are offset from and substantially parallel to one another.
23. A device, as claimed in claim 17, wherein:
said second circuit board lies in a third plane which is offset from and extends substantially parallel to said first and second planes.
24. A device, as claimed in claim 17, wherein:
said second circuit board includes means for digital signal processing enabling the pre-video signal conditioned by said first circuit board to be viewed by said video monitor.
25. A device, as claimed in claim 17, wherein:
said first circuit board converts said pre-video signal to a post video signal for direct reception by a remote video device, said post-video signal being of a format selected from the group consisting of a NTSC/PAL video signal and a VGA video signal.
26. A device, as claimed in claim 17, wherein:
said array of CMOS pixels includes an array of passive CMOS pixels, wherein individual passive CMOS pixels of said array of passive CMOS pixels each include a photo diode for producing photoelectrically generated signals, and an access transistor communicating with said photo diode to control the release of photoelectrically generated signals.
27. A device, as claimed in claim 17, wherein:
individual pixels within said array of CMOS pixels each include an amplifier.
28. A device, as claimed in claim 17, further including:
a retractable cable interconnecting said camera module to said video telephone, said retractable cable enabling said camera module to be pulled away from said video telephone for selective taking of images by said camera module, and allowing said camera module to be stored within said video telephone by retracting said cable and securing said camera module within said video telephone.
29. A device, as claimed in claim 17, wherein:
said video telephone further includes a flip panel hingedly connected thereto, and wherein said video monitor is hingedly connected to said flip panel.
30. A device as claimed in claim 17, further including:
adjustable linkage interconnecting said video monitor to said video telephone.
31. A device, as claimed in claim 17, further including:
a remote video device electrically coupled to said video telephone for further viewing said video images.
32. A device, as claimed in claim 31, wherein:
said remote video device is selected from the group consisting of a television and a computer monitor.

33. A video telephone for conducting telephonic communications including receiving and transmitting video images between two parties of a telephone call, said video telephone comprising:
an image sensor lying in a first plane, and an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of CMOS pixels for timing and control of said array CMOS pixels, said image sensor producing a pre-video signal;
a first circuit board residing on a second plane and electrically communicating with said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;
a camera module housing said image sensor;
a transceiver/amplifier section electrically coupled to said first circuit board for transmitting, reciving, and amplifying video and audio signals;
a digital signal processor electrically coupled to said first circuit board and said transceiver/amplifier section, said digital signal processor further conditioning said pre-vide signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals from said transceiver/amplifier section;
a microphone electrically communicating with said digital signal processor for receiving audio signals;
a speaker electrically communicating with said digital signal processor for broadcasting audio signals;
a video monitor attached to said video phone, said video monitor for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section;
a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video monitor; and
a power supply mounted to said video telephone for providing power thereto.
34. A device, as claimed in claim 33, wherein:
said first circuit board is placed adjacent said image sensor within said camera module.
35. A device, as claimed in claim 33, wherein:
said first circuit board is remote from said image sensor and placed within a housing of said video telephone.
36. A device, as claimed in claim 33, wherein:
said image sensor defines a profile area in said first plane, and said first circuit board is positioned in longitudinal alignment with said image sensor such that said first circuit board does not extend substantially beyond said profile area.
37. A device, as claimed in claim 33, further including:
a second circuit board electrically coupled with said first circuit board and said image sensor for further processing said pre-video signal, said second board being placed adjacent said first circuit board.
38. A device, as claimed in claim 33, wherein:
said first and second planes are offset from and substantially parallel to one another.
39. A device, as claimed in claim 37, wherein:
said second circuit board lies in a third plane which is offset from and extends substantially parallel to said first and second planes.
40. A device, as claimed in claim 37, wherein:
said second circuit board includes means for digital signal processing enabling the pre-video signal conditioned by said first circuit board to be viewed by said video monitor.

41. A device, as claimed in claim 33, wherein:

said first circuit board converts said pre-video signal to a post-video signal for direct reception by a remote video device, said post-video signal being of a format selected from the group consisting of a NTSC/PAL video signal and a VGA video signal.

42. A device, as claimed in claim 33, wherein:

said array of CMOS pixels includes an array of passive CMOS pixels, wherein individual passive CMOS pixels of said array of passive CMOS pixels each include a photo diode for producing photoelectrically generated signals, and an access transistor communicating with said photo diode to control the release of photoelectrically generated signals.

43. A device, as claimed in claim 33, wherein:

individual pixels within said array of CMOS pixels each include an amplifier.

44. A device, as claimed in claim 33, further including:

a retractable cable interconnecting said imaging device to said video telephone, said retractable cable enabling said imaging device to be pulled away from said video telephone for selective taking of images by said imaging device, and allowing said imaging device to be stored within said video telephone by retracting said cable and securing said camera module within said video telephone.

45. A device, as claimed in claim 33, wherein:

said video telephone further includes a flip panel hingedly connected thereto, and wherein said video monitor is hingedly connected to said flip panel.

46. A device as claimed in claim 33, further including:

adjustable linkage interconnecting said video monitor to said video telephone.

47. A device, as claimed in claim 33, further including:

a remote video device electrically coupled to said video system for further viewing said video image.

48. A device, as claimed in claim 47, wherein:

said remote video device is selected from the group consisting of a television and a computer monitor.

49. In a wireless telephone for conducting wireless telephonic communications, the improvement comprising:

a video system integral with said telephone for receiving and transmitting video images, and for viewing said images, said video system comprising:

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically coupled to said image sensor, said first circuit board including circuitry means for timing and control of said array of CMOS pixels and circuitry means for processing and converting said pre-video signal to a desired video format; and

a video monitor attached to said wireless phone for viewing said video images, said video monitor communicating with said first circuit board.

50. A device, as claimed in claim 49, wherein:

said first circuit board is placed adjacent to said image sensor and within said camera module.

51. A device, as claimed in claim 49, wherein:

said first circuit board is remote from said image sensor and placed within a housing of said telephone.

52. In a wireless telephone for conducting wireless telephonic communications, the improvement comprising:

a video system integral with said telephone for receiving and transmitting video images, and for viewing said images, said video system comprising:

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, circuitry means electrically coupled to said array of CMOS pixels for timing and control of said array of CMOS pixels, said circuitry means for timing and control being placed remote from said array of CMOS pixels on a second plane, said image sensor producing a pre-video signal, a first circuit board lying in a third plane and electrically coupled to said image sensor, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format; and

a video monitor attached to said wireless phone for viewing said video images, said video monitor communicating with said first circuit board, and displaying video images processed by said first circuit board.

53. A device, as claimed in claim 52, wherein:

said circuitry means for timing and control is placed adjacent to said image sensor in said camera module.

54. A device, as claimed in claim 52, wherein:

said circuitry means for timing and control is placed within a housing of a telephone.

55. In a video telephone for receiving and transmitting telephone communications to include video signals transmitted by the user of the phone, and video signals received from the party to whom a call is made, the video telephone including a video monitor for viewing the video signals, the improvement comprising:

a camera module for taking video images, said camera module communicating with circuitry within said video telephone enabling viewing on said video telephone and enabling video signals to be transmitted from said camera module by said party for viewing, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically connected to said image sensor, said first circuit board including circuitry means for timing and control of said array of CMOS pixels and circuitry means for processing and converting said pre-video signal to a desired video format.

56. A device, as claimed in claim 55, wherein:

said first circuit board is placed adjacent said image sensor within said camera module.

57. A device, as claimed in claim 55, wherein:

said first circuit board is placed within a housing of said telephone.

58. In a video telephone for receiving and transmitting telephone communications to include video signals transmitted by the user of the phone, and video signals received from the party to whom a call was made, the video telephone including a video monitor for viewing the video signals, the improvement comprising:

a camera module for taking video images, said camera module communicating with circuitry within said video telephone enabling viewing of said video images on said video telephone and enabling video signals to be transmitted from said camera module for viewing by said party, said camera module including an image

sensor housed therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of said CMOS pixels for timing and control of said array of CMOS pixels, said circuitry means for timing and control placed remote from said array of CMOS pixels on a second plane, said image sensor producing a pre-video signal, a first circuit board electrically connected to said image sensor and lying in a third plane, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format.

59. A device, as claimed in claim **58**, wherein:

said circuitry means for timing and control is placed adjacent to said image sensor in said camera module.

60. A device, as claimed in claim **58**, wherein:

said circuitry means for timing and control is placed within a housing of said telephone.

61. A video telephone for conducting telephonic communications including receiving and transmitting video images between two parties of a telephone call, said video telephone comprising:

an image sensor lying in a first plane including an array of CMOS pixels for receiving images thereon, said image sensor producing a pre-video signal;

a first circuit board lying in a second plane electrically communicating with said image sensor, said first circuit board including circuitry means for timing and control of said array of CMOS pixels and circuitry means for processing and converting said pre-video signal to a desired video format;

a camera module housing said image sensor;

a transceiver/amplifier section electrically coupled to said first circuit board for transmitting, receiving, and amplifying video and audio signals;

a digital signal processor electrically coupled to said first circuit board and said transceiver/amplifier section, said digital signal processor further conditioning said pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and auio signals from said transceiver/amplifier section;

a microphone electrically communicating with said digital signal processor for receiving audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video monitor attached to said video phone, and video monitor for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section;

a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video monitor; and

a power supply mounted to said video telephone for providing power thereto.

62. A device, as claimed in claim **61**, wherein:

said first circuit board is placed adjacent to said image sensor and within said camera module.

63. A device, as claimed in claim **61**, wherein:

said first circuit board is remote from said image sensor, and placed within a housing of said telephone.

64. A video telephone for conducting telephonic communications including receiving and transmitting video images between two parties of a telephone call, said video telephone comprising:

an image sensor lying in a first plane, and an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of CMOS pixels for timing and control of said array of CMOS pixels, said circuitry means for timing and control being placed remote from said array of CMOS pixels on a second plane, said image sensor producing a pre-video signal;

a first circuit board electrically coupled with said image sensor and lying in a third plane, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format;

a camera module housing said image sensor;

a transceiver/amplifier section electrically coupled to said first circuit board for transmitting, receiving, and amplifying video and audio signals;

a digital signal processor electrically coupled to said first circuit board and said transceiver/amplifier section, said digital signal processor further conditioning said pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals from said transceiver/amplifier section;

a microphone electrically communicating with said digital signal processor for receiving audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video monitor attached to said video phone, said video monitor for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section;

a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video monitor; and

a power supply mounted to said video telephone for providing power thereto.

65. A device, as claimed in claim **64**, wherein:

said circuitry means for timing and control is placed adjacent to said image sensor in said camera module.

66. A device, as claimed in claim **65**, wherein:

said circuitry means for timing and control is placed within a housing of said telephone.

67. In a method for conducting video telephone communications with a video telephone, the improvement comprising the steps of:

providing a camera module having an image sensor housed therein;

providing a flexible cable for interconnecting the camera module to the video telephone;

displacing the camera module away from the video telephone;

pointing the camera module at a targeted object, the flexible cable bending in response to the pointing action; and

taking video images of the targeted object by the camera module for viewing on the video telephone, and for transmission of the video images to another party.

68. A method, as claimed in claim **67**, further comprising the steps of:

selectively extending and selectively retracting the cable, enabling the camera module to be pointed in a desired direction toward the targeted object.

69. A method, as claimed in claim **67**, wherein:

said image sensor includes a CMOS pixel array.

70. In a wireless telephone for conducting wireless telephonic communications, the improvement comprising:

a camera module housing an image sensor therein, said camera module for producing video images of a targeted object;

means for interconnecting said camera module to said wireless telephone, said means for interconnecting being flexible enabling said camera module to be selectively displaced at a location remote from said wireless telephone; and

a video monitor attached to said wireless phone for selectively viewing video images taken by said camera module, and for selectively viewing incoming video images transmitted by another party.

71. A device, as claimed in claim **70**, wherein:

said video telephone includes a housing, and an opening for receiving said camera module so as to place said camera module in a stored position.

72. In a video telephone for receiving and transmitting audio and visual communications to include video signals transmitted by the user of the video telephone, and video signals received from the party to whom a call was made, the video telephone including a housing, and a video monitor for viewing the transmitted and incoming video signals, the improvement comprising:

a camera module housing an image sensor therein, said camera module for producing video images of a targeted object; and

means for interconnecting said camera module to said wireless telephone, said means for interconnecting being flexible enabling said camera module to be selectively displaced at a location remote from said wireless telephone.

73. A device, as claimed in claim **72**, wherein:

said video telephone includes a housing, and an opening for receiving said camera module so as to place said camera module in a stored position.

74. In a video telephone for conducting communications including receiving and transmitting video images between two parties of a video telephone call, the improvement comprising:

a camera module housing an image sensor therein;

circuitry means coupled to said image sensor for timing and control of said image sensor;

circuitry means for processing images taken by said image sensor to create video signals of a desired video format;

means for interconnecting said camera module to a housing of said video telephone, said means for interconnecting being flexible enabling said camera module to be selectively displaced from said housing by the user for pointing the camera module at a targeted object.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,452,626 B1
DATED : September 17, 2002
INVENTOR(S) : Edwin L. Adair

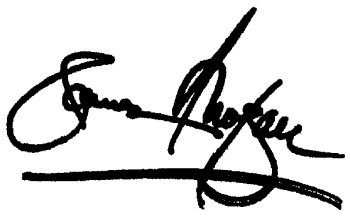
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 24,
Line 26, add claim 75 as follows:

75. A device, as claimed in claim 74, wherein:
said video telephone includes a housing, and an opening for receiving said camera module so as to place said camera module in a stored position.

Signed and Sealed this

Thirteenth Day of May, 2003



JAMES E. ROGAN
Director of the United States Patent and Trademark Office

US007002621B2

(12) **United States Patent**
Adair et al.

(10) **Patent No.: US 7,002,621 B2**
(45) **Date of Patent: Feb. 21, 2006**

(54) **COMMUNICATION DEVICES INCORPORATING REDUCED AREA IMAGING DEVICES**

(76) Inventors: **Edwin L. Adair**, 317 Paragon Way, Castle Pines Village, CO (US) 80104; **Jeffrey L. Adair**, 1861 E. Redfox Pl., Highlands Ranch, CO (US) 80126; **Randall S. Adair**, 3082 S. Flamingo Way, Denver, CO (US) 80222

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 759 days.

(21) Appl. No.: **09/934,201**

(22) Filed: **Aug. 21, 2001**

(65) **Prior Publication Data**

US 2002/0089589 A1 Jul. 11, 2002

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/613,027, filed on Jul. 10, 2000, which is a continuation-in-part of application No. 09/496,312, filed on Feb. 1, 2000, now Pat. No. 6,275,255, which is a continuation of application No. 09/175,685, filed on Oct. 20, 1998, now Pat. No. 6,043,839, which is a continuation-in-part of application No. 08/944,322, filed on Oct. 6, 1997, now Pat. No. 5,929,901.

(51) **Int. Cl.**
H04Q 7/32 (2006.01)

(52) **U.S. Cl.** **348/158**; 455/556

(58) **Field of Classification Search** 348/65–76, 348/155–159, 373–376, 60–400; 455/556–566, 455/400–600

See application file for complete search history.

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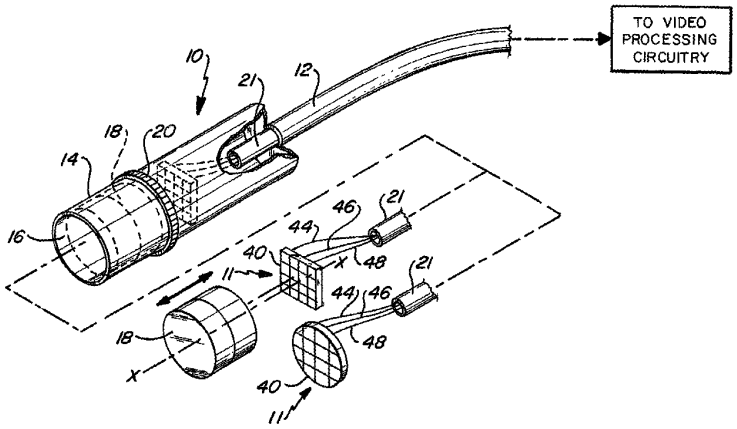
Primary Examiner—Andy Rao
(74) *Attorney, Agent, or Firm*—Sheridan Ross PC

(57) **ABSTRACT**

A reduced area imaging device is provided for use with a communication device, such as a wireless/cellular phone. Various configurations of the imaging device are provided which locate the elements of the imaging device at desired locations. The communication device includes a miniature LCD-type monitor which displays not only images taken by the camera module, but also incoming video messages. The camera module may communicate with the housing of the communication device by wired connection, or wirelessly. The camera module is of such small size that it can be stored within the housing of the communication device. The camera module may be pointed at any object within sight of the user, without having to move the phone housing in order to take video images. Any acceptable wireless standard may be used for wireless communication between the camera module and the video telephone. One particularly advantageous wireless standard includes Bluetooth.

62 Claims, 14 Drawing Sheets



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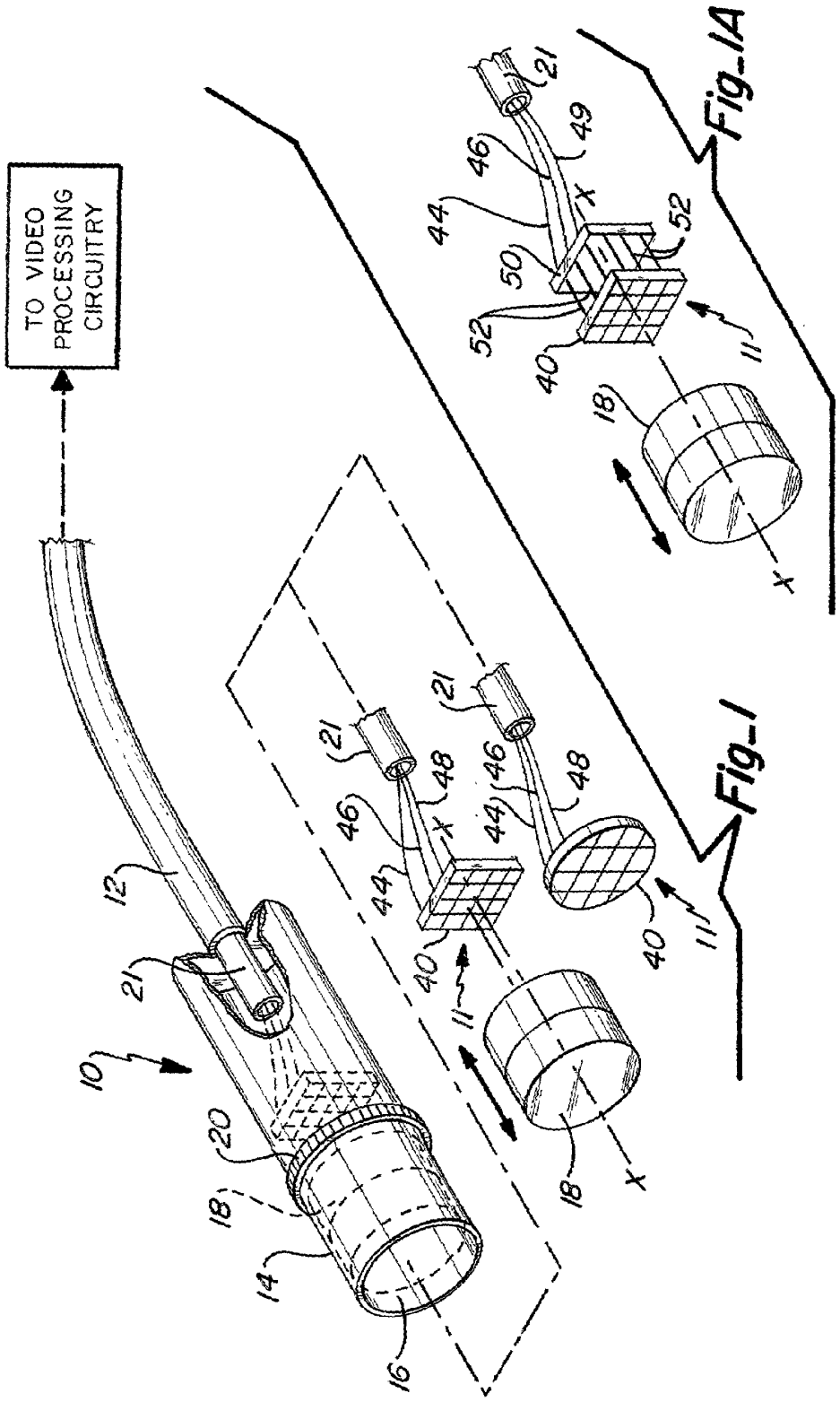
TO VIDEO PROCESSING CIRCUITRY
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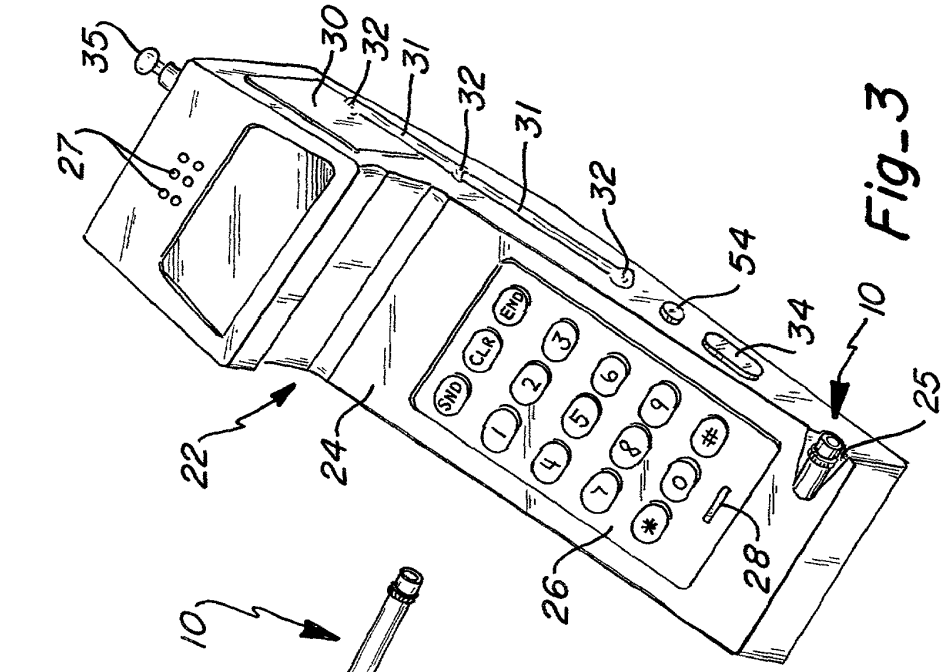
Fig_1
Fig_1A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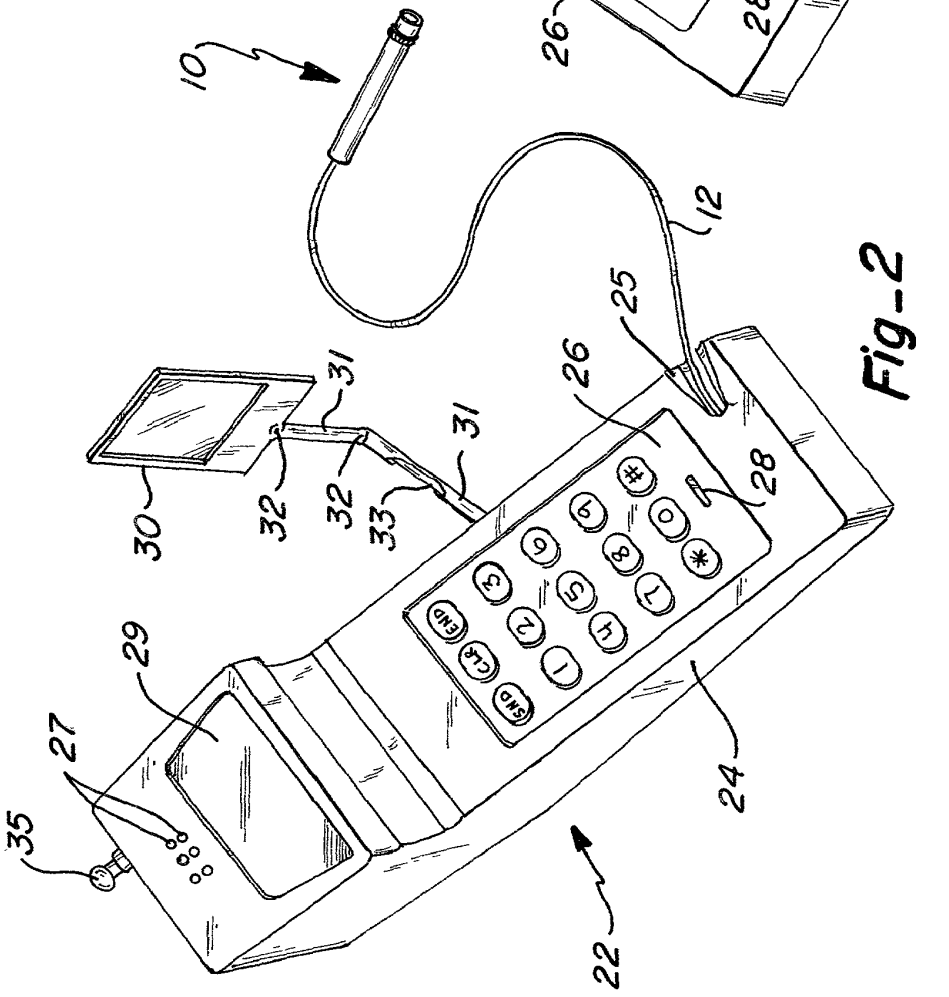
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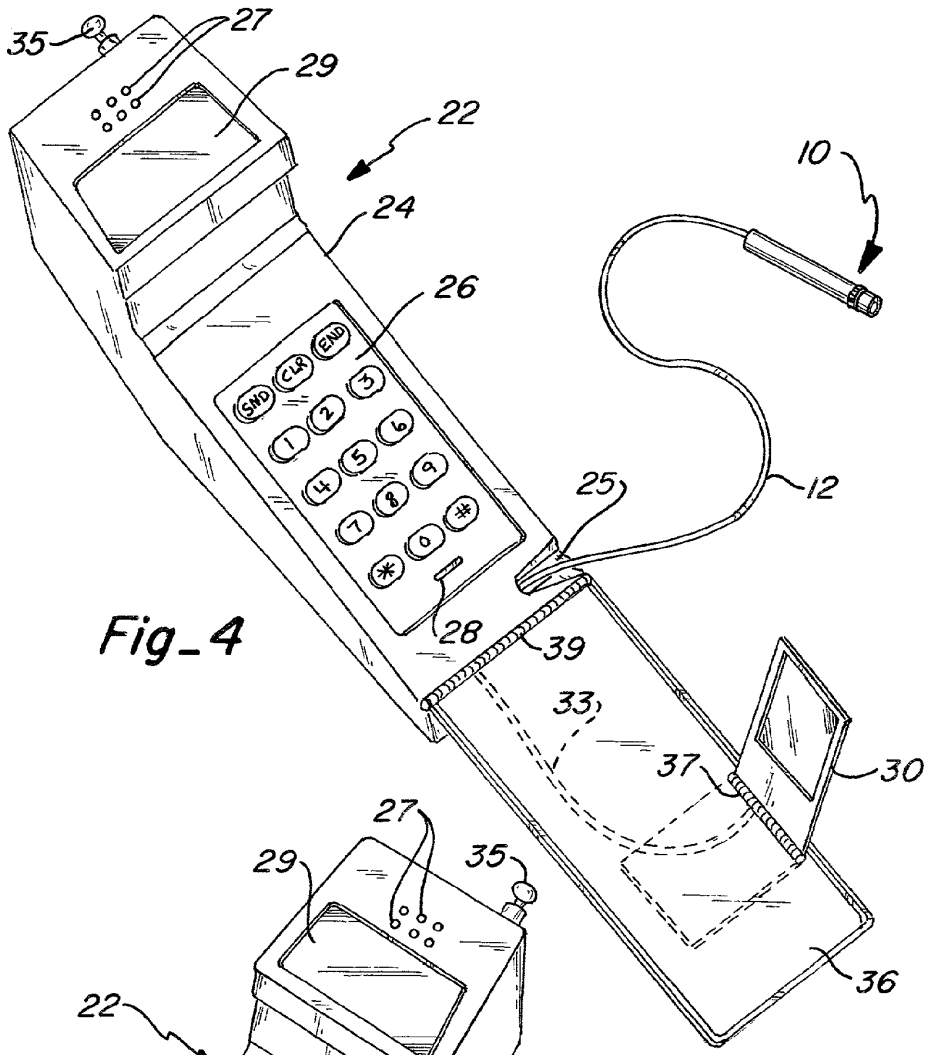
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Fig_4

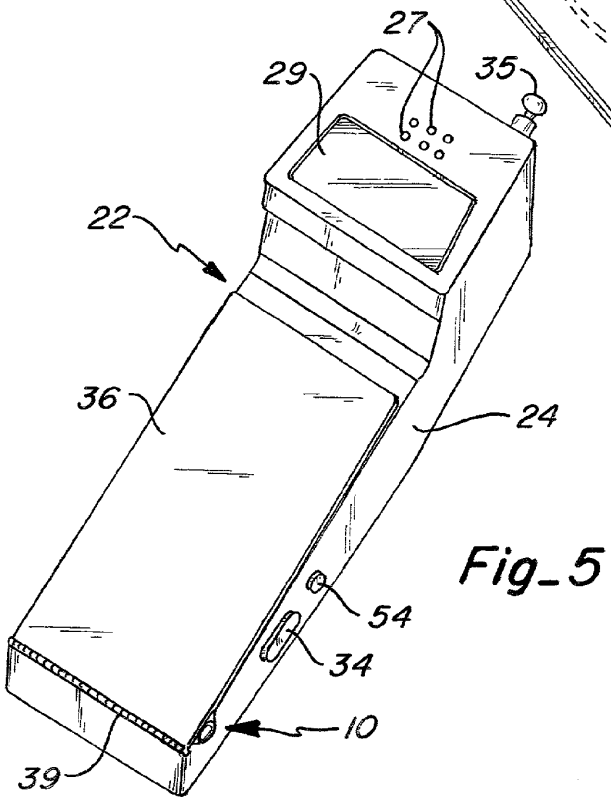
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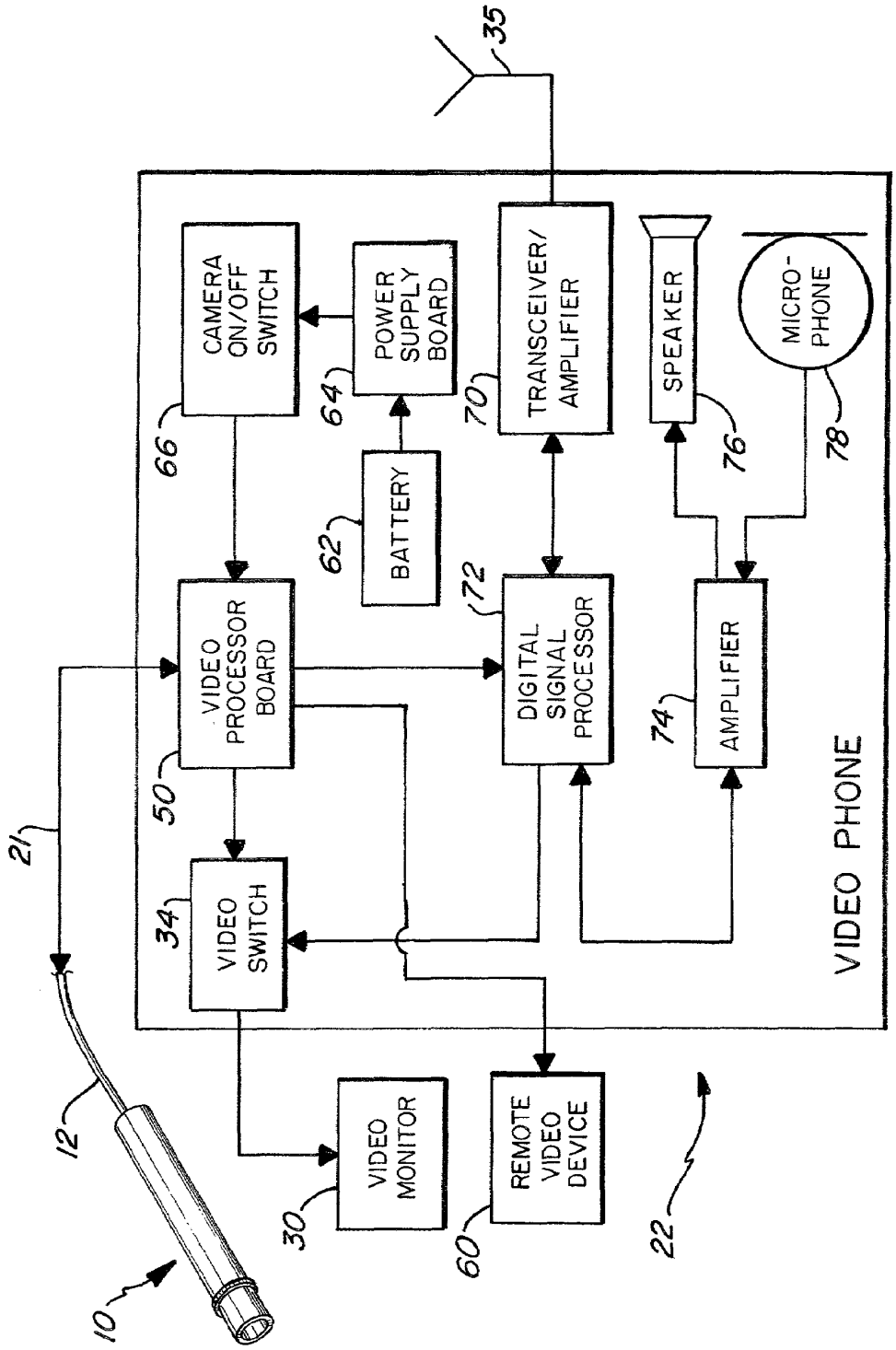
Fig_5


35
CAMERA ON/OFF SWITCH
66
POWER SUPPLY BOARD
64
TRANSCEIVER/ AMPLIFIER
70
SPEAKER
76
MICRO-PHONE
78
BATTERY
62
VIDEO PROCESSOR BOARD
50
DIGITAL SIGNAL PROCESSOR
72
AMPLIFIER
74
VIDEO SWITCH
34
VIDEO PHONE
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12
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VIDEO MONITOR
30
REMOTE VIDEO DEVICE
60
22

Fig_6

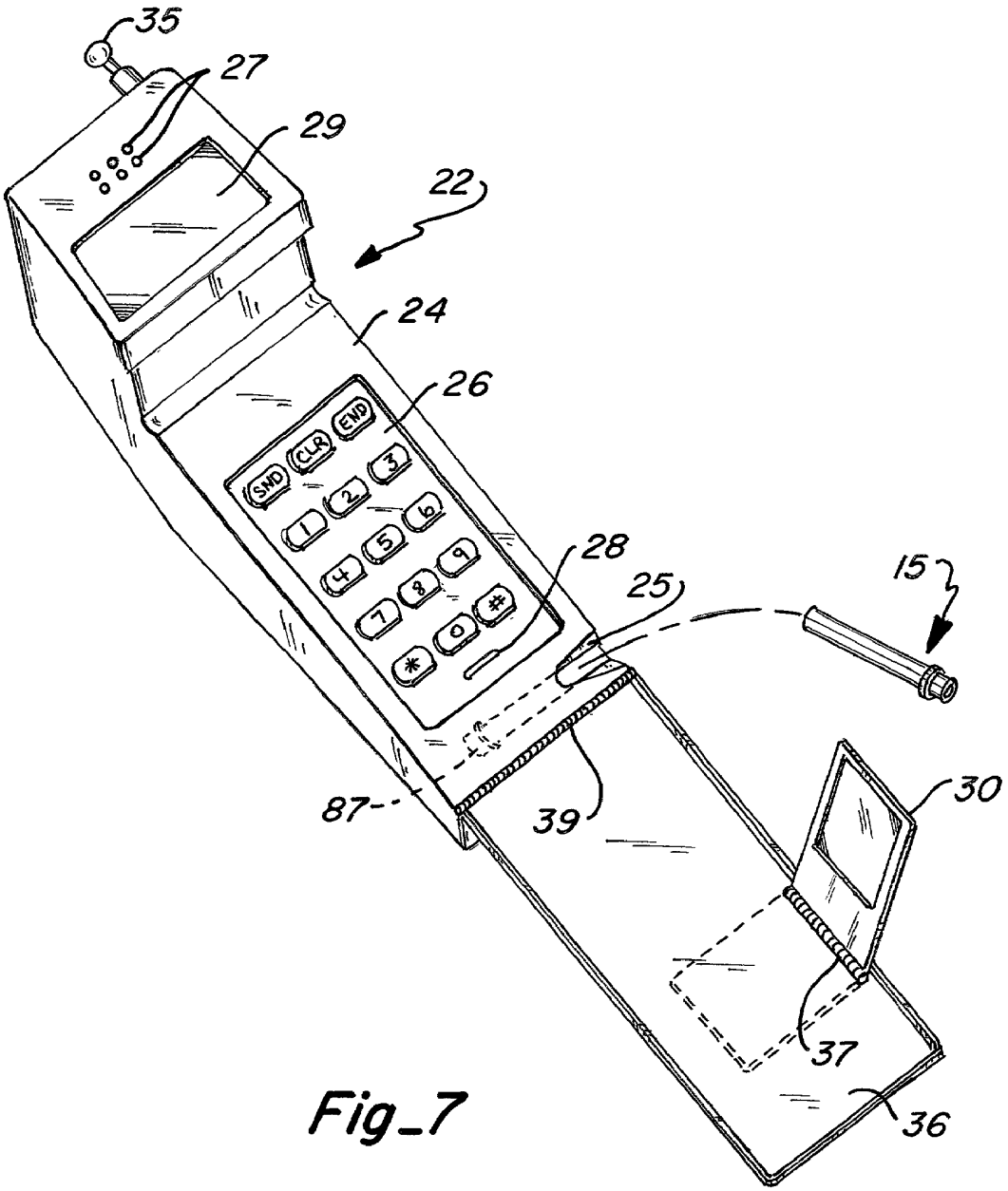
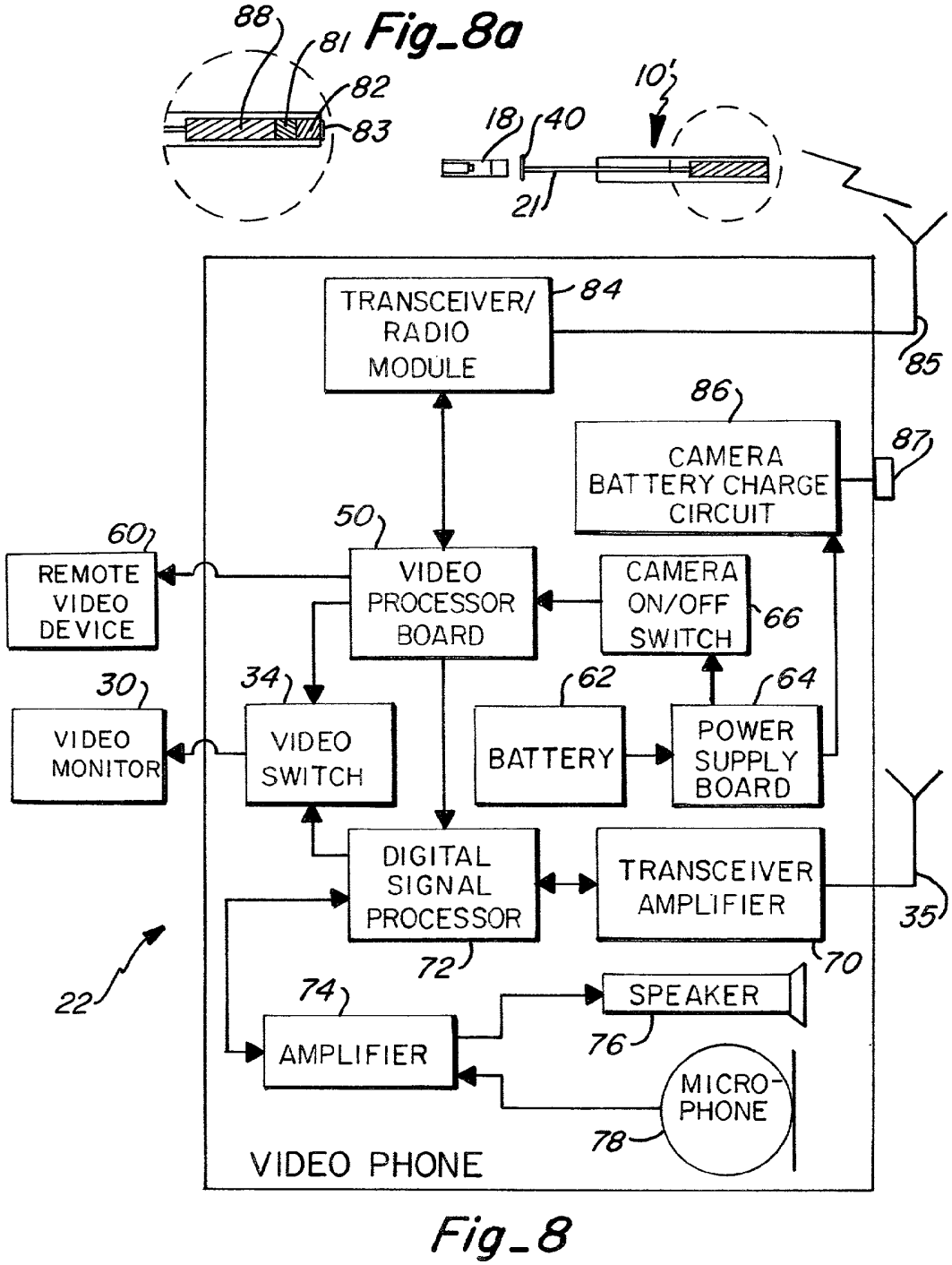


Fig_7


88
81
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TRANSCEIVER/ RADIO MODULE
84
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86
CAMERA BATTERY CHARGE CIRCUIT
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50
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REMOTE VIDEO DEVICE
VIDEO PROCESSOR BOARD
CAMERA ON/OFF SWITCH
66
30
34
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64
VIDEO MONITOR
VIDEO SWITCH
BATTERY
POWER SUPPLY BOARD
DIGITAL SIGNAL PROCESSOR
TRANSCEIVER AMPLIFIER
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MICRO-PHONE
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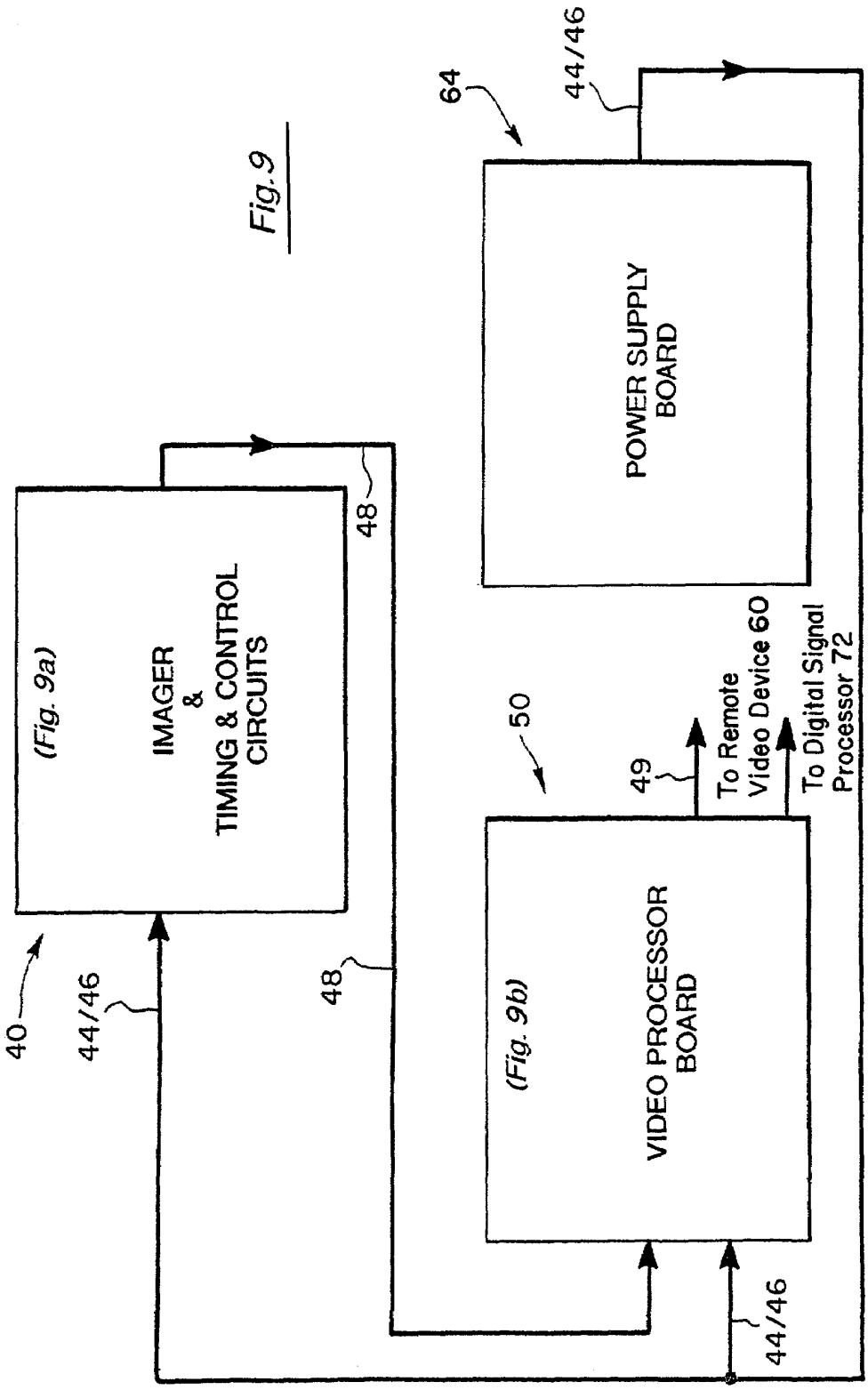
VIDEO PHONE

Fig_8

Fig.9


64
44/46
POWER SUPPLY BOARD
48
(Fig. 9a)
IMAGER & TIMING & CONTROL CIRCUITS
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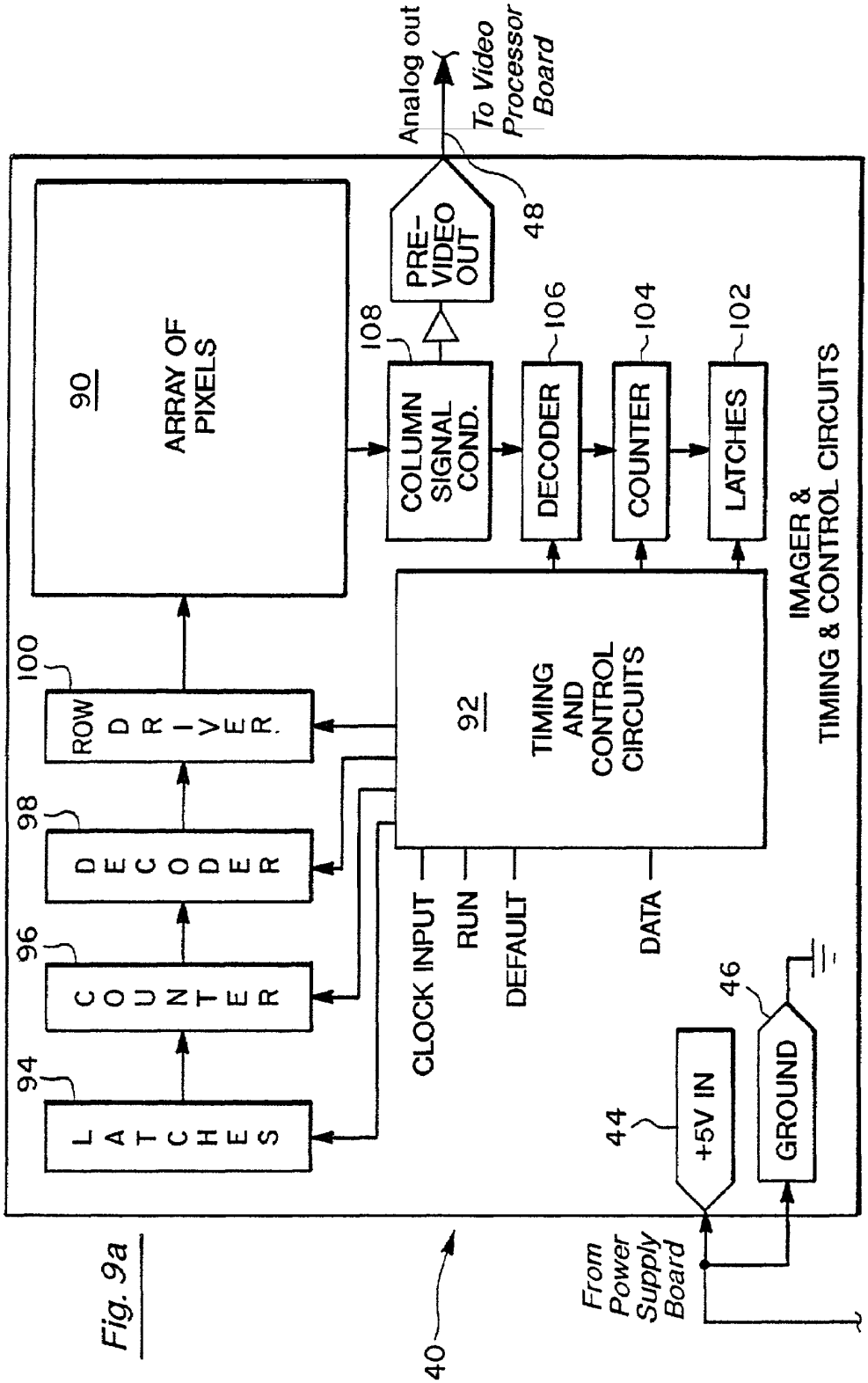
49
To Remote Video Device 60
To Digital Signal Processor 72
40
44/46
48
(Fig. 9b)
VIDEO PROCESSOR BOARD
44/46


Analog out
To Video Processor Board
PRE-VIDEO OUT
48
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ARRAY OF PIXELS
108
COLUMN SIGNAL COND.
106
DECODER
104
COUNTER
102
LATCHES
IMAGER & TIMING & CONTROL CIRCUITS
92
TIMING AND CONTROL CIRCUITS
100
ROW DRIVER
98
DECODER
96
COUNTER
94
LATCHES
CLOCK INPUT
RUN
DEFAULT
DATA
44
+5V IN
46
GROUND
From Power Supply Board
40

Fig. 9a

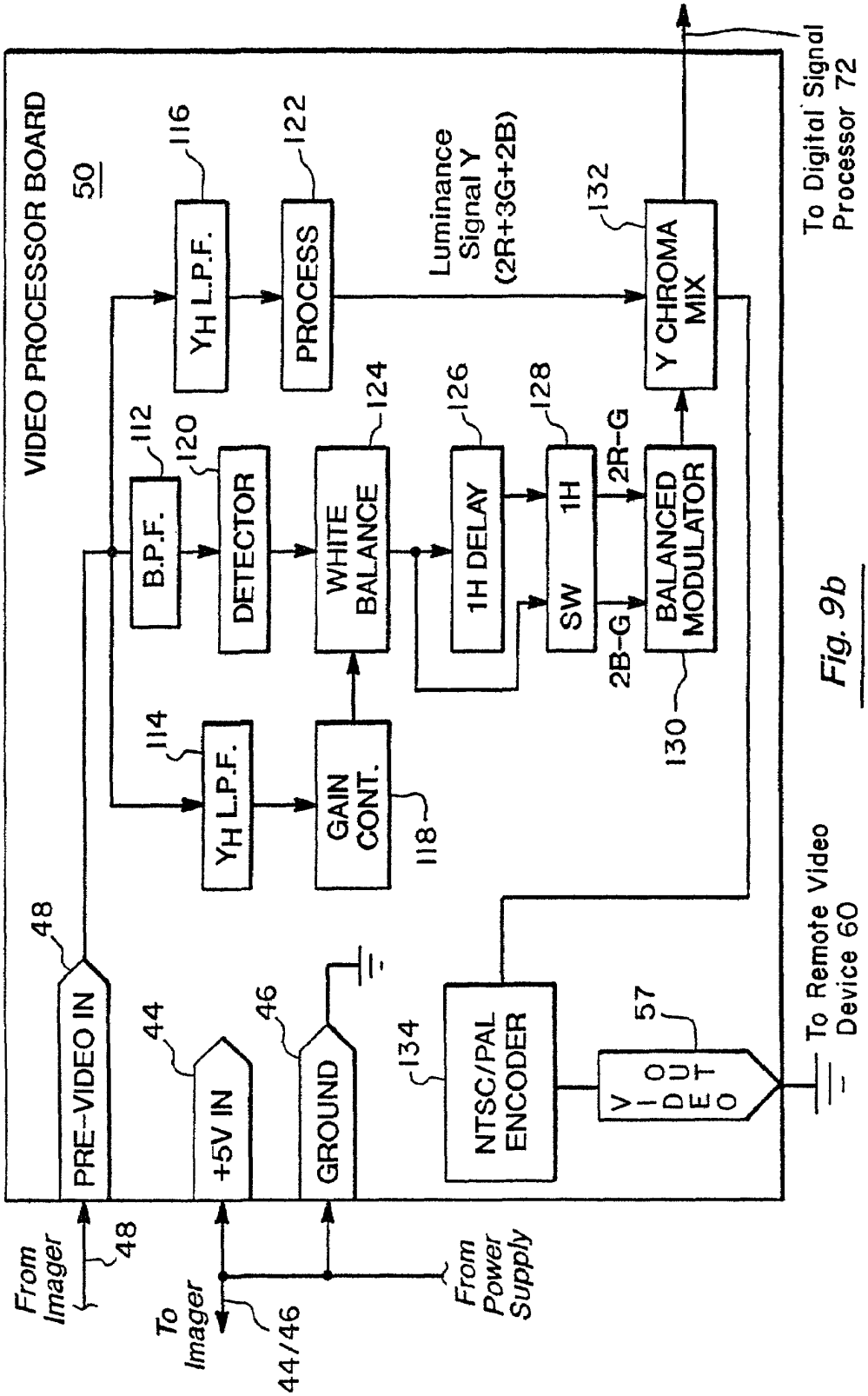

VIDEO PROCESSOR BOARD
50
PRE-VIDEO IN
48
+5V IN
44
GROUND
46
NTSC/PAL ENCODER
134
VIDEO OUT
57
B.P.F.
112
DETECTOR
120
WHITE BALANCE
124
1H DELAY
126
SW 1H
128
BALANCED MODULATOR
Y CHROMA MIX
132
YH L.P.F.
116
PROCESS
122
YH L.P.F.
114
GAIN CONT.
118
Luminance Signal Y (2R+3G+2B)
2R-G
2B-G
130
To Digital Signal Processor 72
To Remote Video Device 60
From Imager
48
To Imager
44/46
From Power Supply

Fig. 9b

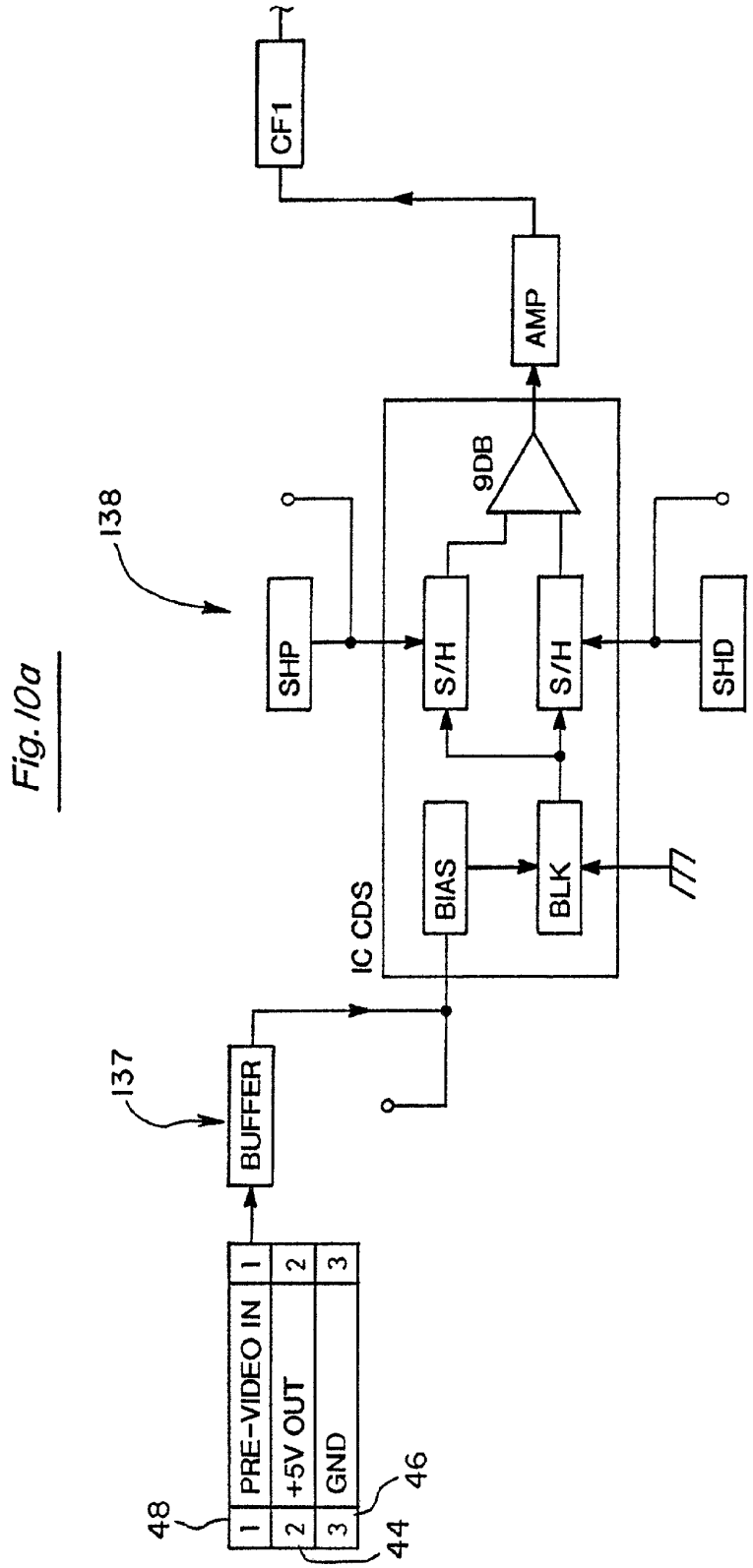

CF1
AMP
9DB
138
SHP
S/H
S/H
SHD
BIAS
BLK
177
IC CDS
137
BUFFER
1
2
3
PRE-VIDEO IN
+5V OUT
GND
48
46
44

Fig. 10a

Fig. 10b

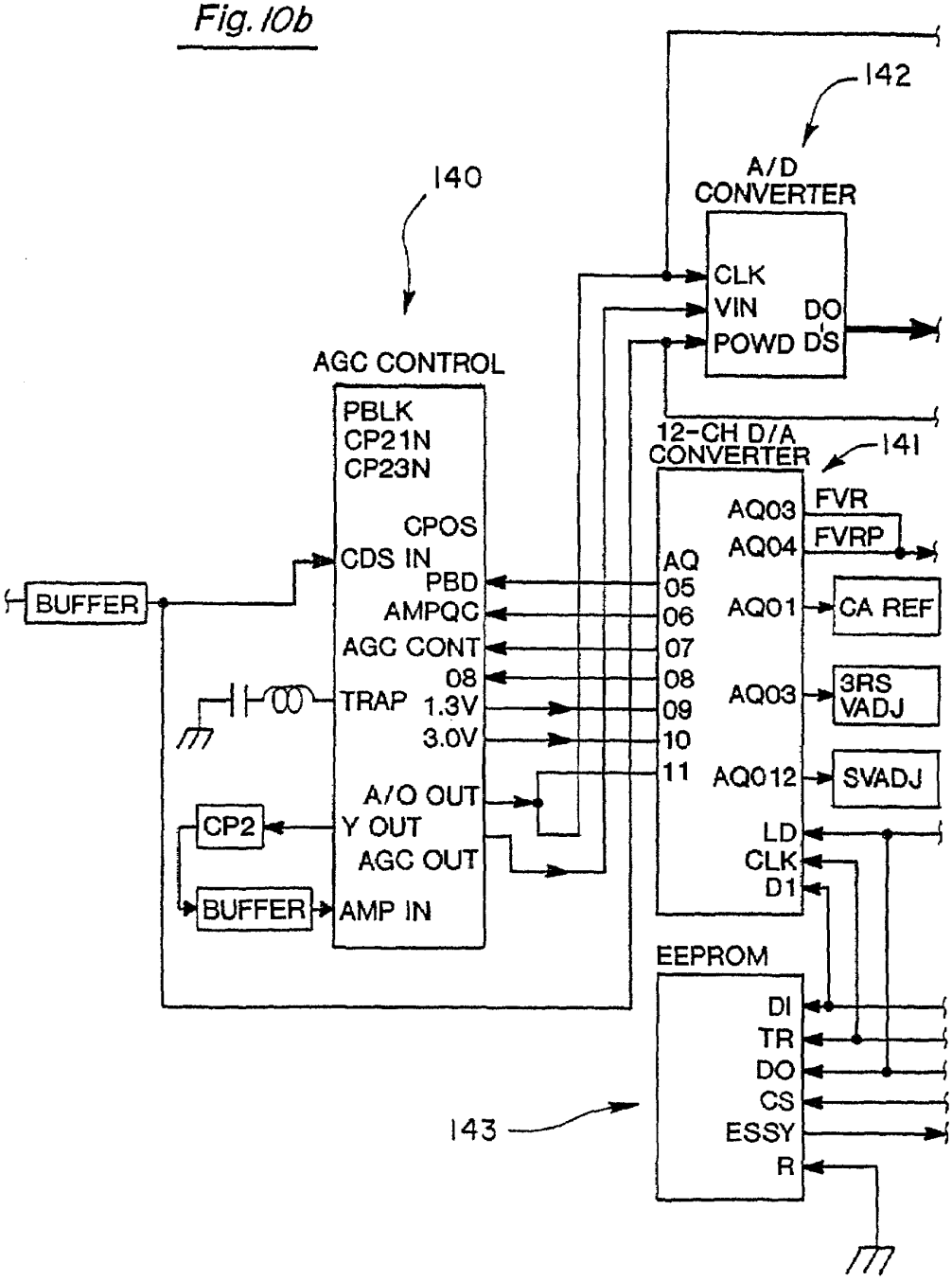
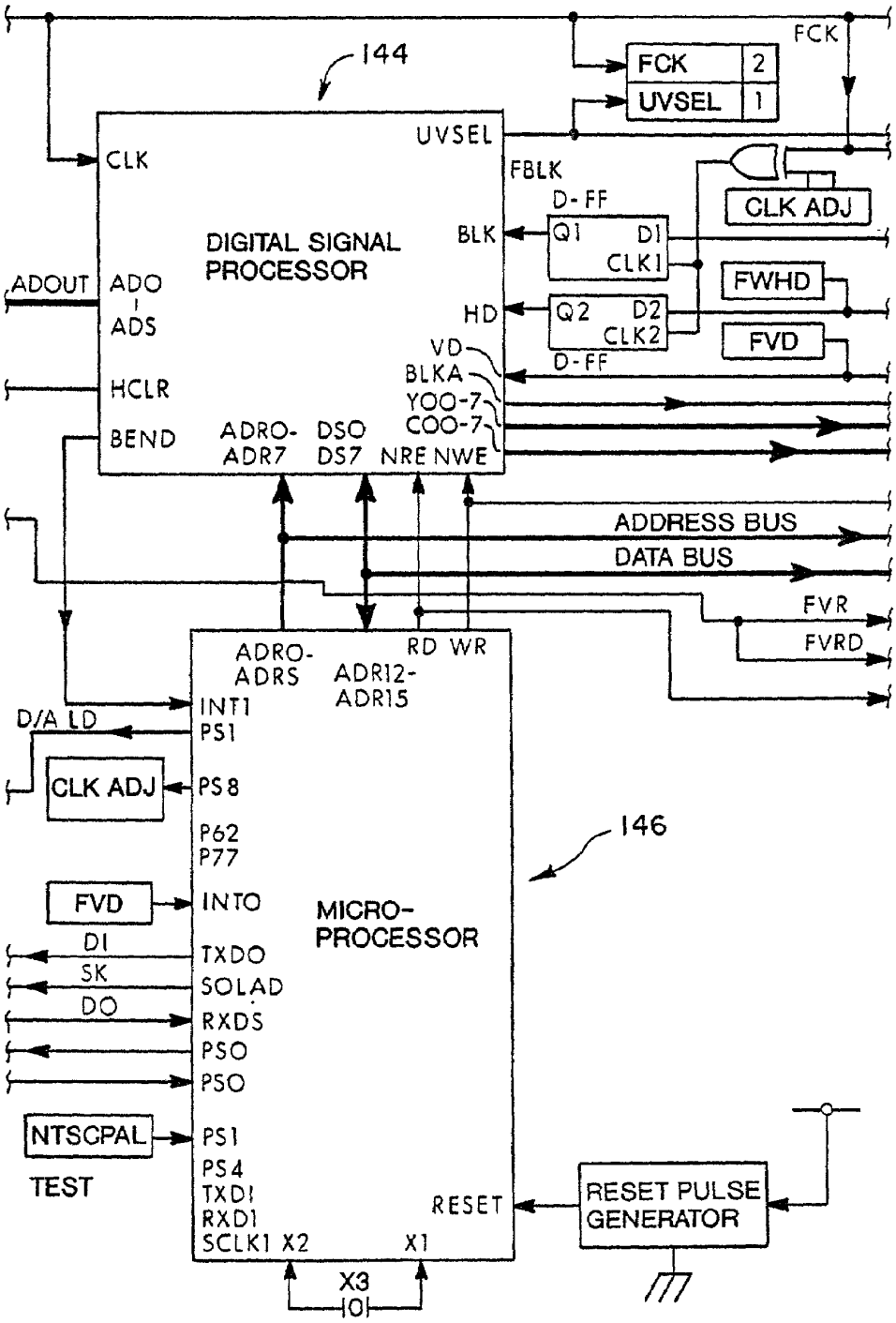

142
A/D CONVERTER
140
CLK
VIN
DO
POWD
DS
AGC CONTROL
PBLK
CP21N
CP23N
12-CH D/A CONVERTER
141
CPOS
CDS IN
PBD
AMPQC
AGC CONT
TRAP
08
1.3V
3.0V
A/O OUT
Y OUT
AGC OUT
AMP IN
BUFFER
CP2
BUFFER
AQ 05
06
07
08
09
10
11
AQ03
AQ04
FVR
FVRP
AQ01
CA REF
AQ03
3RS VADJ
AQ012
SVADJ
LD
CLK
D1
EEPROM
DI
TR
DO
CS
ESSY
R
143

Fig. 10c


144
FCK
FCK 2
UVSEL 1
UVSEL
CLK
FBLK
D-FF
CLK ADJ
DIGITAL SIGNAL PROCESSOR
BLK
Q1 D1
CLK1
FWHD
ADOUT
ADO
ADS
HD
Q2 D2
CLK2
FVD
VD
BLKA
D-FF
HCLR
YOO-7
COO-7
BEND
ADRO-ADR7
DSO DS7
NRE NWE
ADDRESS BUS
DATA BUS
FVR
FVRD
RD WR
ADRO-ADRS
ADR12-ADR15
INT1
PS1
D/A LD
CLK ADJ
PS8
P62
P77
146
FVD
INTO
MICRO-PROCESSOR
DI
TXDO
SK
SOLAD
DO
RXDS
PSO
PSO
NTSCPAL
PS1
PS4
TXD1
RXD1
SCLK1 X2
X1
RESET
RESET PULSE GENERATOR
TEST
X3
10

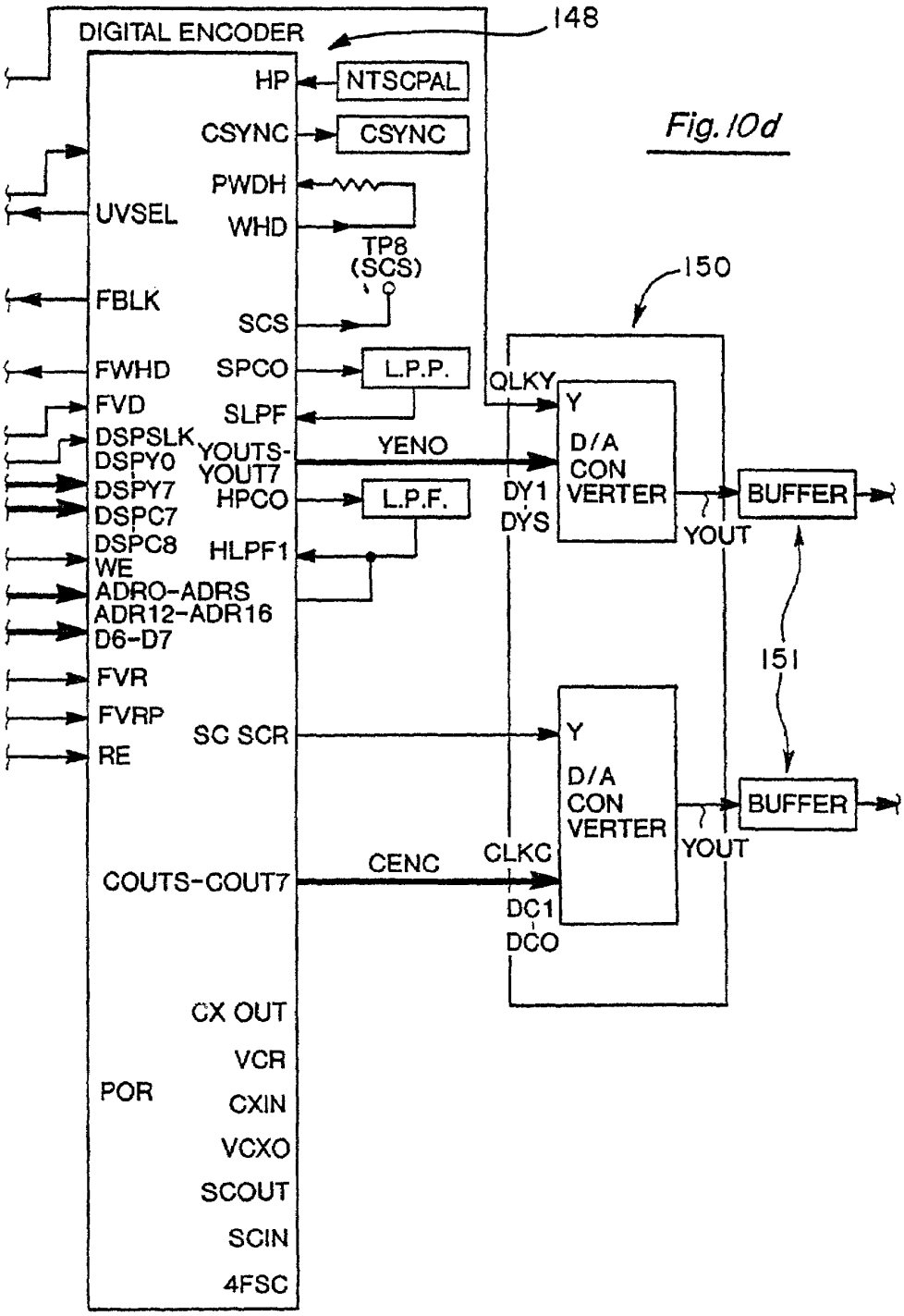

DIGITAL ENCODER
148
HP
NTSCPAL
CSYNC
CSYNC
PWDH
UVSEL
WHD
TP8
(SCS)
FBLK
SCS
150
FWHD
SPCO
L.P.P.
QLKY
FVD
SLPF
Y
DSPSLK
YOUTS-
YOUT7
YENO
D/A
CON
VERTER
DSPY0
DSPY7
DSPC7
HPCO
L.P.F.
DY1
DYS
BUFFER
YOUT
DSPC8
WE
HLPF1
ADRO-ADRS
ADR12-ADR16
D6-D7
151
FVR
FVRP
SC SCR
RE
Y
D/A
CON
VERTER
BUFFER
YOUT
CENC
CLKC
COUTS-COUT7
DC1
DCO
CX OUT
VCR
POR
CXIN
VCXO
SCOUT
SCIN
4FSC

Fig. 10d

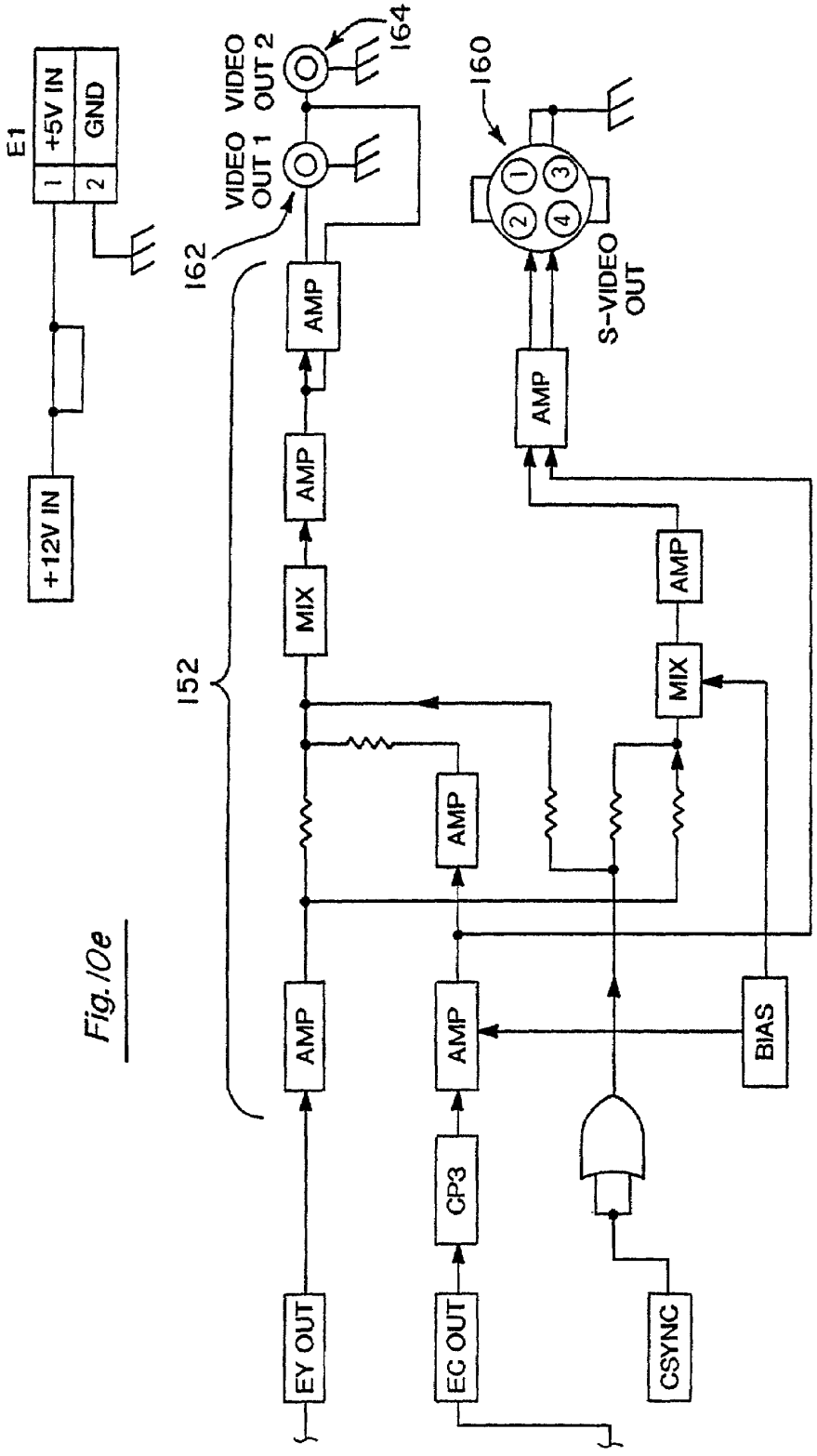

E1
+5V IN
GND
1
2
+12V IN
VIDEO OUT 2
VIDEO OUT 1
164
162
160
S-VIDEO OUT
AMP
MIX
152
BIAS
CP3
EY OUT
EC OUT
CSYNC

Fig. 10e

COMMUNICATION DEVICES INCORPORATING REDUCED AREA IMAGING DEVICES

This application is a continuation-in-part of U.S. patent application Ser. No. 09/613,027 filed on Jul. 10, 2000 entitled "Communication Devices Incorporating Reduced Area Imaging Devices", which is a continuation in part of U.S. Ser. No. 09/496,312, filed Feb. 1, 2000 now U.S. Pat. No. 6,275,255, and entitled "Reduced Area Imaging Devices", which is a continuation application of U.S. Ser. No. 09/175,685, filed Oct. 20, 1998 and entitled "Reduced Area Imaging Devices", now U.S. Pat. No. 6,043,839, which is a continuation-in-part of U.S. Ser. No. 08/944,322, filed Oct. 6, 1997 and entitled "Reduced Area Imaging Devices Incorporated Within Surgical Instruments", now U.S. Pat. No. 5,929,901.

TECHNICAL FIELD

This invention relates to solid state image sensors and associated electronics, and more particularly, to solid state image sensors which are configured to be of a minimum size and used within communication devices specifically including video telephones.

BACKGROUND ART

The three most common solid state image sensors include charged coupled devices (CCD), charge injection devices (CID) and photo diode arrays (PDA). In the mid-1980s, complementary metal oxide semiconductors (CMOS) were developed for industrial use. CMOS imaging devices offer improved functionality and simplified system interfacing. Furthermore, many CMOS imagers can be manufactured at a fraction of the cost of other solid state imaging technologies.

The CCD device is still the preferred type of imager used in scientific applications. Only recently have CMOS-type devices been improved such that the quality of imaging compares to that of CCD devices. However, there are enormous drawbacks with CCD devices. Two major drawbacks are that CCD device have immense power requirements, and the amount of processing circuitry required for a CCD imager always requires the use of a remote processing circuitry module which can process the image signal produced by the CCD imager. Also, because of the type of chip architecture used with CCD devices, on-chip processing is impossible. Therefore, even timing and control circuitry must be remoted from the CCD imager plane. Therefore, CCD technology is the antithesis of "camera on a chip" technology discussed below.

One particular advance in CMOS technology has been in the active pixel-type CMOS imagers which consist of randomly accessible pixels with an amplifier at each pixel site. One advantage of active pixel-type imagers is that the amplifier placement results in lower noise levels. Another major advantage is that these CMOS imagers can be mass produced on standard semiconductor production lines. One particularly notable advance in the area of CMOS imagers including active pixel-type arrays is the CMOS imager described in U.S. Pat. No. 5,471,515 to Fossum, et al. This CMOS imager can incorporate a number of other different electronic controls that are usually found on multiple circuit boards of much larger size. For example, timing circuits, and special functions such as zoom and anti-jitter controls can be placed on the same circuit board containing the CMOS pixel array without significantly increasing the overall size of the host circuit board. Furthermore, this particular CMOS imager requires 100 times less power than a CCD-type imager. In short, the CMOS imager disclosed in Fossum, et al. has enabled the development of a "camera on a chip."

Passive pixel-type CMOS imagers have also been improved so that they too can be used in an imaging device which qualifies as a "camera on a chip." In short, the major difference between passive and active CMOS pixel arrays is that a passive pixel-type imager does not perform signal amplification at each pixel site. One example of a manufacturer which has developed a passive pixel array with performance nearly equal to known active pixel devices and being compatible with the read out circuitry disclosed in the U.S. Pat. No. 5,471,515 is VLSI Vision, Ltd., 1190 Saratoga Avenue, Suite 180, San Jose, Calif. 95129. A further description of this passive pixel device may be found in applicant's patent entitled "Reduced Area Imaging Devices Incorporated Within Surgical Instruments," U.S. Pat. No. 5,986,693, and is hereby incorporated by reference.

In addition to the active pixel-type CMOS imager which is disclosed in U.S. Pat. No. 5,471,515, there have been developments in the industry for other solid state imagers which have resulted in the ability to have a "camera on a chip." For example, Suni Microsystems, Inc. of Mountain View, Calif., has developed a CCD/CMOS hybrid which combines the high quality image processing of CCDs with standard CMOS circuitry construction. In short, Suni Microsystems, Inc. has modified the standard CMOS and CCD manufacturing processes to create a hybrid process providing CCD components with their own substrate which is separate from the P well and N well substrates used by the CMOS components. Accordingly, the CCD and CMOS components of the hybrid may reside on different regions of the same chip or wafer. Additionally, this hybrid is able to run on a low power source (5 volts) which is normally not possible on standard CCD imagers which require 10 to 30 volt power supplies. A brief explanation of this CCD/CMOS hybrid can be found in the article entitled "Startup Suni Bets on Integrated Process" found in *Electronic News*, Jan. 20, 1997 issue. This reference is hereby incorporated by reference for purposes of explaining this particular type of imaging processor.

Another example of a recent development in solid state imaging is the development of a CMOS imaging sensor which is able to achieve analog to digital conversion on each of the pixels within the pixel array. This type of improved CMOS imager includes transistors at every pixel to provide digital instead of analog output that enable the delivery of decoders and sense amplifiers much like standard memory chips. With this new technology, it may, therefore, be possible to manufacture a true digital "camera on a chip." This CMOS imager has been developed by a Stanford University joint project and is headed by Professor Abbas el-Gamal.

A second approach to creating a CMOS-based digital imaging device includes the use of an over-sample converter at each pixel with a one bit comparator placed at the edge of the pixel array instead of performing all of the analog to digital functions on the pixel. This new design technology has been called MOSAD (multiplexed over sample analog to digital) conversion. The result of this new process is low power usage, along with the capability to achieve enhanced dynamic range, possibly up to 20 bits. This process has been developed by Amain Electronics of Simi Valley, Calif. A brief description of both of the processes developed by Stanford University and Amain Electronics can be found in

an article entitled "A/D Conversion Revolution for CMOS Sensor?," September 1998 issue of *Advanced Imaging*. This reference is also hereby incorporated by reference for purposes of explaining these particular types of imaging processors.

Yet another example of a recent development with respect to solid state imaging is an imaging device developed by ShellCase, of Jerusalem, Israel. In an article entitled "A CSP Optoelectronic Package for Imaging and Light Detection Applications" (A. Badihi), ShellCase introduces a die-sized, ultrathin optoelectronic package which is completely packaged at the wafer level using semiconductor processing. In short, ShellCase provides a chip scale package (CSP) process for accepting digital image sensors which may be used, for example, in miniature cameras. The die-sized, ultrathin package is produced through a wafer level process which utilizes optically clear materials and completely encases the imager die. This packaging method, ideally suited for optoelectronic devices, results in superior optical performance and form factor not available by traditional image sensors. This reference is also incorporated by reference for purposes of explaining ShellCase's chip scale package process.

Yet another example of a recent development with respect to solid state imaging is shown in U.S. Pat. No. 6,020,581 entitled "Solid State CMOS Imager Using Silicon on Insulator or Bulk Silicon." This patent discloses an image sensor incorporating a plurality of detector cells arranged in an array wherein each detector cell as a MOSFET with a floating body and operable as a lateral bipolar transistor to amplify charge collected by the floating body. This reference overcomes problems of insufficient charge being collected in detector cells formed on silicon on insulator (SOI) substrates due to silicon thickness and will also work in bulk silicon embodiments.

The above-mentioned developments in solid state imaging technology have shown that "camera on a chip" devices will continue to be enhanced not only in terms of the quality of imaging which may be achieved, but also in the specific construction of the devices which may be manufactured by new breakthrough processes.

Although the "camera on a chip" concept is one which has great merit for application in many industrial areas, a need still exists for a reduced area imaging device which can be used in even the smallest type of industrial application. Recently, there have been developments with providing camera capabilities for wireless/cellular phones. Two-way still image video phones are making appearances on the market now. Additionally, there has been information regarding various worldwide manufacturers who are soon to come out with fully functional two-way video in combination with wireless/cellular phones. Because it is desirable to have a wireless/cellular phone of minimum size and weight, it is also desirable to have supporting imaging circuitry which is also of minimum size and weight. Accordingly, the invention described herein is ideal for use with upcoming video phone technology.

It is one object of this invention to provide a reduced area imaging device incorporated within a communication device which takes advantage of "camera on a chip" technology, but rearrange the circuitry in a selective stacked relationship so that there is a minimum profile presented when used within a communication device.

It is yet another object of this invention to provide imaging capability for a communication device wherein the camera used is of such small size that it can be attached to the communication device by a retractable cord which enables the imaging device to be used to image anything to which the camera is pointed at by the user without having to move the communication device away from the mouth when speaking.

It is yet another object of this invention to provide a camera with a communication device wherein the camera communicates with the communications device by a wireless link such as an RF radio link so that the camera does not have to be physically connected to the communications device. This wireless connection further enhances the capability to use the camera to shoot video without having to move the communication device or otherwise manipulate the communication device in a manner which detracts from shooting the video.

In all applications, to include use of the imaging device of this invention with a communication device, "camera on a chip" technology can be improved with respect to reducing its profile area, and incorporating such a reduced area imaging device within a communication device such that minimal size and weight is added to the communication device, and further that the imaging device can be used to image selected targets by the user.

DISCLOSURE OF THE INVENTION

In accordance with the present invention, reduced area imaging devices are provided in combination with a communication device such as a wireless/cellular phone. The term "imaging device" as used herein describes the imaging elements and processing circuitry which is used to produce a video signal which may be accepted by both a standard video device such as a television or video monitor accompanying a personal computer, and a small LCD screen which is incorporated within the video phone. The term "image sensor" as used herein describes the components of a solid state imaging device which captures images and stores them within the structure of each of the pixels in the array of pixels found in the imaging device. As further discussed below, the timing and control circuits can be placed either on the same planar structure as the pixel array, in which case the image sensor can also be defined as an integrated circuit, or the timing and control circuitry can be placed remote from the pixel array. The terms "video signal" or "image signal" as used herein, and unless otherwise more specifically defined, refer to an image which at some point during its processing by the imaging device, is found in the form of electrons which have been placed in a specific format or domain. The term "processing circuitry" as used herein refers to the electronic components within the imaging device which receive the image signal from the image sensor and ultimately place the image signal in a usable format. The terms "timing and control circuits" or "timing and control circuitry" as used herein refer to the electronic components which control the release of the image signal from the pixel array.

In a first embodiment of the communication device, the imaging device connects to the communication device by a cable or cord which may retract within the housing of the communication device. Thus in this embodiment, the camera is tethered to the communication device. In a second embodiment, the imaging device does not have to be physically connected to the imaging device; rather, a wireless RF link or other acceptable wireless technology is used so that video signals produced by the imaging device may be transmitted to and received by the communications device. One particularly advantageous wireless technology usable with the communications device of this invention is known as "Bluetooth". Another recent wireless technology which is

usable with the invention is a wireless protocol known as "IEEE 802.15.3". This wireless standard is developing under the joint efforts of Kodak, Motorola, Cisco and the International Electronic and Electrical Engineers Standards Association (IEEE) Wireless Personal Area Network Working Group (WPAN). Bluetooth technology provides a universal radio interface in the 2.4 GHz frequency band that enables portable electronic devices to connect and communicate wirelessly via short-range ad hoc networks. Bluetooth radios operate in an unlicensed Instrumentation, Scientific, Medical (ISM) band at 2.4 GHz. Bluetooth is a combination of circuit and packet switching. Slots can be reserved for synchronous packets. Each packet is transmitted in a different hop frequency. A packet nominally covers a single slot, but can be extended to cover up to five slots. Bluetooth can support an asynchronous data channel, up to three simultaneous synchronous voice channels, or a channel that simultaneously supports asynchronous data and synchronous voice. Spectrum spreading is used to facilitate optional operation at power levels up to 100 mW worldwide. Spectrum spreading is accomplished by frequency hopping in 79 hops displaced by 1 MHZ, staring at 2.402 GHz and stopping at 2.480 GHz. the maximum frequency-hopping rate is 1600 hops per second. The nominal link range is 10 centimeters to 10 meters, but can be extended to more than 100 meters by increasing the transmit power. A shaped, binary FM modulation is applied to minimize transceiver complexity. The gross data rate is 1 Mb/second. A time division duplex scheme is used for full-duplex transmission. Additional technical information describing the Bluetooth global specification is found on the world wide web at www.bluetooth.com. Additional information regarding the technical specification for the IEEE 802.15.3 standard may be found at http://www. ieee802.org/15, under the link for Task Force Three (TG3).

In a first arrangement of the imaging device, the image sensor, with or without the timing and control circuitry, may be placed at the distal tip of a very small video camera module which is attached by a cable or cord to the communication device, or the camera module communicates with the communication device by a wireless RF link while the remaining processing circuitry may be placed within the housing of the communication device.

In a second arrangement of the imaging device, the image sensor and the processing circuitry may all be placed in a stacked arrangement of miniature circuit boards and positioned at the distal tip of the video camera module. In this second arrangement, the pixel array of the image sensor may be placed by itself on its own circuit board while the timing and control circuitry and processing circuitry are placed on one or more other circuit boards, or the circuitry for timing and control may be placed with the pixel array on one circuit board, while the remaining processing circuitry can be placed on one or more of the other circuit boards.

In yet another alternative arrangement of the imaging device, the pixel array, timing and control circuits, and some of the processing circuitry can be placed near the distal end of the video camera module with the remaining part of the processing circuitry being placed in the housing of the communication device.

For the arrangement or configuration of the imaging device which calls for the array of pixels and the timing and control circuitry to be placed on the same circuit board, only one conductor is required in order to transmit the image signal to the video processing circuitry. When the timing and control circuits are incorporated onto other circuit boards, a plurality of connections are required in order to connect the timing and control circuitry to the pixel array, and then the one conductor is also required to transmit the image signal to the video processing circuitry.

The invention disclosed herein can also be considered an improvement to a cellular/wireless phone wherein the improvement comprises a video system. The video system would include the video monitor attached to the phone, the camera module, the imaging device within the camera module, as well as supporting video processing circuitry for the imaging device. In yet another aspect, the invention disclosed herein can also be considered an improvement to a video telephone wherein the improvement comprises a novel imaging device, preferably of CMOS construction. For this improvement comprising the imaging device, the imaging device includes the array of pixels, and the supporting video processing circuitry for providing a video ready signal. In yet another aspect, the invention disclosed herein can also be considered an improvement to a video telephone wherein the improvement comprises an imaging device which utilizes a wireless standard in order to transmit video images to the video telephone.

The video ready signal produced by the video processing circuitry may be of differing video formats for viewing on different types of video devices. For example, the video ready signal may be a NTSC/PAL compatible video signal for viewing on a remote video device such as a TV; the video signal may be a YUV 4:2:2 signal for viewing on a video monitor attached to the phone; and/or the video signal may be VGA compatible for viewing on a personal computer. Accordingly, the invention disclosed herein has utility with respect to an overall combination of elements, as well as various sub-combination of elements.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an enlarged fragmentary partially exploded perspective view of the distal end of the camera module which is used in conjunction with the communication device, specifically illustrating the arrangement of the image sensor with respect to the other elements of the camera module;

FIG. **1***a* is an enlarged exploded perspective view illustrating another configuration of the image sensor wherein video processing circuitry is placed behind and in longitudinal alignment with the image sensor;

FIG. **2** is a perspective view of the communication device in a first embodiment incorporating the reduced area imaging device of this invention, and further illustrating the video monitor in operation, along with the camera module pulled out in the extended position;

FIG. **3** illustrates the communication device of FIG. **2** wherein the camera module is in the retracted position, along with the video monitor in the folded or retracted position;

FIG. **4** is another perspective view of the communication device of this invention in the first embodiment illustrating an alternative arrangement for placement of the video monitor within a flip panel;

FIG. **5** is a perspective view of the communication device of FIG. **4** illustrating the alternative arrangement of the video monitor with the video monitor stored within the folded flip panel;

FIG. **6** is an overall schematic diagram of the functional electronic components in the first embodiment which make up both the communication device, and the reduced area imaging device;

FIG. **7** is a perspective view of the communication device in a second embodiment wherein the camera module utilizes

a wireless technology, thus the camera module may be physically separated from the communication device during operation, but can still be housed within the communication device for storage and for recharge of the battery of the camera module;

FIG. **8** is an overall schematic diagram, similar to FIG. **6**, of the functional components which make up the communication device and a simplified cross sectional view of the camera module in the second preferred embodiment wherein the camera module communicates with the communication device via a wireless link;

FIG. **8***a* is an enlarged view of some of the components of the camera module, specifically, the components used in the wireless link with the communication device;

FIG. **9** is a more detailed schematic diagram of the functional electronic components which make up the imaging device;

FIG. **9***a* is an enlarged schematic diagram of a circuit board/planar structure which may include the array of pixels and the timing and control circuitry;

FIG. **9***b* is an enlarged schematic diagram of a video processing board/planar structure having placed thereon the processing circuitry which processes the pre-video signal generated by the array of pixels and which converts the pre-video signal to a post-video signal which may be accepted by an NTSC/PAL compatible video device; and

FIGS. **10***a*–**10***e* are schematic diagrams that illustrate an example of specific circuitry which may be used to make the video processing circuitry of the imaging device.

BEST MODE FOR CARRYING OUT THE INVENTION

In accordance with the invention, as shown in FIG. **1**, a camera module **10** is provided which incorporates a reduced area imaging device **11**. As further discussed below, the elements of the imaging device **11** may all be found near one location, or the elements may be separated from one another and interconnected by the appropriate wired connections. The array of pixels making up the image sensor captures images and stores them in the form of electrical energy by conversion of light photons to electrons. This conversion takes place by the photo diodes in each pixel which communicate with one or more capacitors which store the electrons. Specifically, the camera module **10** includes an outer tube/sheath **14** which houses the components of the imaging device. The camera module is shown as being cylindrical in shape having a window **16** sealed at the distal end of the camera module. A retractable cable **12** extends from the proximal end of the camera module **10**. A shielded cable **21** is used to house the conductors which communicate with the imaging device **11**. The shielded cable **21** is then housed within the retractable cable **12**. A lens group **18** is positioned at the distal end of the camera module to enable an image to be appropriately conditioned prior to the image impinging upon the imaging device **11**. Also shown is a focusing ring **20** which enables the lens group **18** to be displaced distally or proximally to best focus an image on the imaging device **11**.

Now referring to FIGS. **2**–**5**, a video phone **22** in a first embodiment is shown which incorporates the camera module **10**. In basic terms, the video phone is simply a standard wireless/cellular phone which has added thereto the ability to send and receive video signals which may both be viewed on video monitor **30**. Beginning first with a description of the basic components of the video phone, it includes a phone housing **24** which holds the components of the video phone. Cable **12** is housed within the housing **24** when in the retracted position. A spring biased spool (not shown) or some other known retracting device is mounted within the housing **24** enabling the cable **12** to be extended or retracted. When the cable is retracted, the camera module **10** can be stored within cavity or opening **25** at the base of housing **24**. This cavity or opening **25** can substantially conform to the size and shape of the camera module **10**. The camera module **10** is illustrated as being elongate and cylindrical, minimizing its size and profile, and enhancing its ability to be stored within opening **25**. As shown in FIG. **3**, when the camera module **10** is stored, it does not increase the overall size of the video telephone **22**, and does not protrude away from the phone housing **24**, thus making the camera module **10** a component which truly integrates with the housing **24** of the video phone **22**. The cable **12** is of a selected length which allows the user to point the camera module **10** toward a targeted object to taking video. A keypad **26** is provided enabling a user to dial the phone, or achieve other well-known telephone functions. An audio receiving assembly **27** in the conventional manner is provided which allows the user to listen to incoming audio. This assembly may later be referred to simply as a speaker. An orifice or hole **28** is provided which communicates with a microphone (discussed below) for transmitting audio signals. The phone display **29** displays the various functions of the phone as controlled by a user. The display **29** in most wireless/cellular phones is a liquid crystal display. The video monitor **30** attaches to the housing **24** as by linkage **31**. As shown, two pieces of linkage are provided, along with three ball/socket type joints **32** which enable the video monitor to be articulated to the desired position with respect to the housing **24**. An internal video cable **33** having a plurality of conductors (not shown) extends through the linkage **31** and the ball and socket joints **32** for providing the video signals which are displayed on the video monitor **30**. The video monitor **30** may be a liquid crystal display (LCD) type, or any other well-known display device of high resolution which has low power requirements, and has minimum size requirements as well. An example of a manufacture of such a miniature LCD monitor includes DISPLAYTECH of Longmont, Colo. DISPLAYTECH manufactures a miniature reflective display that consists of ferroelectric liquid crystal (FLC) applied to a CMOS integrated circuit. The reflective display is a VGA display panel having low voltage digital operation, low power requirements, and full color operation. One of their specific products includes the LightCasterÔ VGA Display Panel, Model LDP-0307-MV1. This is but one example of an LCD monitor which is available and usable within the invention herein described. As further discussed below, a video select switch **34** is mounted on the housing **24** which enables a user to select viewing of either incoming video signals, or to view the outgoing video signals which are those images taken by the camera module **10**. A conventional antenna **35** is provided to enhance reception and transmission capabilities of the video phone.

FIGS. **4** and **5** illustrate a modification of the video phone of FIGS. **2** and **3**. Specifically, FIGS. **4** and **5** illustrate an alternative way in which to attach the video monitor **30** to the video phone **22**. As shown, FIGS. **4** and **5** illustrate a flip panel **36** which attaches to the base of the housing **24** as by hinge **39**. The video monitor itself is then mounted to the flip panel **36** as by hinge **37**. Video signals are transmitted to the video monitor **30** of FIGS. **4** and **5** by the conductors housed in video cable **33**. As shown, video cable **33** is routed through the flip panel **36**. The video monitor **30** of FIGS. **4**

and **5** can be placed in the desired position by rotating the flip panel **36** about hinge **39**, and then rotating the video monitor **30** about hinge **37**.

Referring back to FIGS. **1** and **1***a*, the imaging device **11** includes an image sensor **40**. FIG. **1** illustrates that the image sensor **40** can be a planar and square shaped member, or alternatively, planar and circular shaped to better fit within outer tube **14**. In the configuration of the imaging device in FIGS. **1** and **1***a*, there are only three conductors which are necessary for providing power to the image sensor **40**, and for transmitting an image from the image sensor **40** back to the processing circuitry found within the phone housing **24**. Specifically, there is a power conductor **44**, a grounding conductor **46**, and an image signal conductor **48**, each of which are hardwired to the image sensor **40**. Thus, shielded cable **21** may simply be a three conductor, **50** ohm type cable.

Image sensor **40** can be as small as 1 mm in its largest dimension. However, a more preferable size for most video phone applications would be between 4 mm to 8 mm in the image sensor's largest dimension (height or width). The image signal transmitted from the image sensor **40** through conductor **48** is also herein referred to as a pre-video signal. Once the pre-video signal has been transmitted from image sensor **40** by means of conductor **48**, it is received by video processing board **50**, as shown in FIG. **6**. Video processing board **50** then carries out all the necessary conditioning of the pre-video signal and places it in a form, also referred to herein as a video ready signal, so that it may be viewed directly on a remote video device such as a television or standard computer video monitor. In order for the pre-video signal to be viewed on the monitor **30**, the pre-video signal is further conditioned by a digital signal processor **72**, as further discussed below. The video signal produced by the video processing board **50** which is viewable by an NTSC/PAL compatible video device (such as a television) can be further defined as a post-video signal.

FIG. **1** illustrates an arrangement wherein the image sensor **40** is placed by itself adjacent the distal end of the camera module **10**. Alternatively, some or all of the video processing circuitry may be placed in adjacent circuit boards directly behind the image sensor **40**.

Accordingly, FIG. **1***a* illustrates video processor board **50** aligned directly behind the image sensor **40**. A plurality of pin connectors **52** can be used to interconnect image sensor **40** to video processor board **50**. Depending upon the specific configuration of image sensor **40**, pin connectors **52** may be provided for structural support and/or to provide a means by which image signals are transmitted between image sensor **40** and board **50**. Additionally, digital signal processor **72** could also be placed behind image sensor **40** and behind video processing board **50**. Accordingly, the image sensor, and all supporting video processing circuitry could be placed at the distal end of the camera module **10**. However, because of the ample space within housing **24**, it may be preferable to place at least some of the video processing circuitry within housing **24**. In the case of FIG. **1***a*, the conductor **49** represents the conductor which may carry the post-video signal for direct connection with a remote video device **60** such as a television or computer monitor. As also discussed further below with respect to the first embodiment, placement of the digital signal processor **72** at the distal tip of the camera module behind the video processing board **50** would also enable yet another conductor (not shown) to connect directly to the video monitor **30** for transmitting a video ready signal to the video monitor **30**.

Again referring to FIG. **1**, the area which is occupied by image sensor **40** may be defined as the profile area of the imaging device and which determines its critical dimensions. If it is desired to place video processing circuitry adjacent the image sensor **40** at the distal end of the camera module **10**, such circuitry must be able to be placed on one or more circuit boards which are longitudinally aligned with image sensor **40** along longitudinal axis XX. If it is not important to limit the size of the profile area, then any circuitry placed behind image sensor **40** can be aligned in an offset manner, or may simply be larger than the profile area of image sensor **40**. In the configuration shown in FIG. **1***a*, it is desirable that elements **40** and **50** be approximately the same size so that they may uniformly fit within the distal end of outer tube **14**.

Now referring to the first embodiment of FIG. **6**, a further explanation is provided of the basic electronic components of the video phone **22** which combines circuitry and functionality of a standard mobile/wireless phone and a video system. One example of a patent disclosing basic mobile phone technology including a discussion of basic phone circuitry is U.S. Pat. No. 6,018,670. This patent is hereby incorporated by reference in its entirety for purposes of disclosing standard or basic mobile phone technology and supporting circuitry. As shown in FIG. **6**, a conventional cellular phone battery **62** is provided which communicates with power supply board **64**. Power supply board **64** conditions various power outputs to the components of the device, to include power to the video components. In the preferred imaging device of this invention, the power to the imaging device may simply be direct current of between about 1.5 to 12 volts, depending upon the power requirements of the imaging device. A camera on/off switch **66** is set to the "on" position in order to activate the camera module **10**. The video processor board **50** then transfers power to supplies the camera module **10**, and also receives the analog pre-video signal back from the camera module, as further discussed below. After processing of the pre-video signal at the video processor board **50**, the video signal is video ready, meaning that it may then be directly viewed on a remote compatible video device **60**, such as a television or computer monitor. The video processor board **50** in FIGS. **6** and **8** is shown as residing within the housing **24**; however, as discussed above with respect to the various arrangements of the imaging device, it can also be located within the distal tip of the camera module. A video port **54** can be provided on the housing **24** enabling a user to take a standard video jack and interconnect the video phone with the video port of the remote video device. The video format for such remote video devices includes NTSC/PAL and VGA; thus, the video signal processed by video processor board **50** creates the video ready signals for use with these remote video devices. For purposes of viewing images on the monitor **30**, the pre-video signal is further processed into a digital format within video processor board **50**, preferably an 8 bit composite video signal format that is commonly referred to as "YUV 4:2:2." This video format easily lends itself to video compression. This 8 bit digital video signal is then sent to the digital signal processor **72** which performs two functions relevant to the video signal. The digital signal processor **72** further converts the signal into a format that is compatible with the driver circuitry of the video monitor **30**. Secondly, the digital signal processor **72** compresses the YUV signal using a common video compression format, preferably JPEG. The JPEG encoded video signal is then mixed with the audio signal created by microphone **78** and amplifier **74**, and the resulting high frequency carrier signal may then be

passed onto the transceiver/amplifier section **70** for transmission. The transceiver/amplifier section also modulates the carrier signal prior to transmission. Depending upon the position of video switch **34**, the video signal from digital signal processor **72** is either sent to the monitor **30**, or is sent to the transceiver/amplifier section **70** for transmission. As also shown, the antenna **35** is used for enhancement of reception and transmission of transmitted and received carrier signals.

The transceiver/amplifier section **70** also serves as a receiver which receives an incoming carrier signal. This incoming signal is then demodulated within section **70**, the video and audio components of the incoming signal are separated, and then these separated signals are then sent to the digital signal processor **72** which performs video decompression. Then, the decompressed video signal is sent to the monitor **30** for viewing (if the video switch **34** is placed in that selected mode). The decompressed audio signal is sent to the amplifier **74**, and then to the speaker **76**. The video switch **34** may simply be a momentary, spring loaded, push button-type switch. When the video switch **34** is not depressed, incoming video, which is received via the handset antenna **35**, is processed as discussed above in the transceiver/amplifier section **70** and digital signal processor **72**, and then sent to the monitor **30**. When the video switch **34** is depressed and held, the video signal produced from the camera module **10** is processed as discussed above, and ultimately sent to the monitor **30**. An operator can cycle the switch **34** between the two positions in order to selectively choose whether to view incoming or outgoing video.

To summarize the operation of the video telephone, a user wishing to contact another party would dial the telephone in the conventional manner. Assuming the party called has video telephone capability, the user could view the images transmitted from the other party by not depressing the video switch **34**. If the user desires to transmit video images to the other party, the user would grasp the camera module **10**, and extend the cord **12** of the camera module by pulling it away from the video telephone, and then point the camera module at the object/person targeted. The user then depresses the video switch **34** which results in transmission of the images captured by the camera module **10** to the other party. Also, the video monitor **30** will display the images captured by the camera module **10** by depressing the video switch **34**. Because the camera module is tethered to the video telephone by retractable cable **12**, the user can continue a conversation with the other party without having to physically remove the video telephone away from the user's mouth when simultaneously taking video by the camera module. Because of the extremely small size of the camera module **10**, it is easily housed within the housing **24** when not in use.

Now referring to FIG. **7**, the second embodiment of the communication device is illustrated which utilizes a wireless camera module **10'**. As with the first embodiment, the camera module **10'** is cylindrical shaped and can be stored within hole or orifice **25**.

Thus, exteriorly, the communication device **22** appears the same, along with camera module **10'** with the exception that there is no cable or cord interconnecting the camera module **10'** to the communication device **22**. Now also referring to FIGS. **8** and **8***a*, in lieu of a wired connection, the camera module **10'** communicates with the communication device **22** by a transceiver radio element **88** which is mounted in the proximal end of the module **10'**. Similarly, the communication device **22** also includes its own transceiver radio module **84** which allows video signals transmitted by transceiver **88** to be received and then passed on to the video processor board **50** for further video signal processing, as necessary. Antennae **85** communicates with transceiver module **84** for enhancing reception of incoming video signals from the camera module **10'**. The camera module **10'** also has its own antennae **81** which enhances reception for authenticating signals which may be transmitted by transceiver **84**. As understood by those skilled in the art, Bluetooth and other RF standards involve two-way communications whereby transmissions are authenticated and synchronized. Thus the transceiver module **84** whose main function is to receive a signal from the camera module **10'**, also transmits some signals to the camera module **10'** and camera module **10'** also acts as a receiver to authenticate and receive such signals. The proximal end of the camera module **10'** also includes a rechargeable battery **82** which is recharged when the module **10'** is seated within the opening **25** of the communication device **22**. The battery **82** can be a common rechargeable nickel-cadmium or lithium-ion type battery. The battery **82** has a contact **83** protruding from the proximal tip of the camera module **10'**. The deepest portion of chamber/opening **25** also has a contact **87** (shown schematically in FIG. **7**) which makes contact with contact **83** when the camera module **10'** is placed in the chamber. Contact **87** electrically couples with camera battery charging circuit **86** which provides an electrical charge for recharging the battery **82**. When the camera module **10'** is placed in the chamber **25**, the external housing or casing of the camera module **10'** is electrically conductive and contacts a ground such as spring loaded clip (not shown) within the chamber **25**. Thus, recharge of the battery **82** can be accomplished.

As shown in FIG. **7**, the charge circuit **86** receives power from power supply board **64**. Thus, the battery **62** of the communication device also provides recharging capability to the battery **82**.

The operation of the communication device is essentially the same in the second embodiment. If the user desires to transmit video images to another party, the user would grasp the camera module **10'**, remove it from chamber **25**, and then point it at the target. The camera module **10'** collects the video images through the objective lens group **18** which conditions images received by the image sensor **40**. The plurality of conductors housed in the shielded miniature cable **21** transfers the video signals to the transceiver radio element **88**. The transceiver radio element **88**, among other functions, adds a high frequency carrier signal and baseband protocol to the video signal which is then transmitted to the transceiver radio module **84**. The video signal transmitted by the transceiver radio element **88** is authenticated by the transceiver radio module **84**, the video signal is stripped of its carrier, and then routed by a link controller (not shown as a separate element apart from transceiver **84**) to the video processor circuitry **50**. The video signal is then handled in the same manner as the first embodiment. The user would depress the video switch **34** to initiate transmission of the video to the other party of the telephone call. Once the camera module **10'** is removed from its seated position in the chamber **25**, the contact between contacts **83** and **87** is broken. This break in electrical contact would allow the battery **82** to energize the camera module **10'**, and thus allow the camera module **10'** to begin wirelessly communicating with the transceiver radio module **84**. The user would be able to easily hold and point the camera module **10'** with one hand, while operating the communication device **22** in the other hand. As with the first embodiment, the video monitor **30** would display the video images simultaneously while video images were being transmitted to the other party so

long as video switch **34** was depressed. If the user wished to receive video images transmitted from the other party, the user would simply reset the video switch **34** to its off or inactive state. The camera module **10'** would continue to shoot video and communicate with the module **84**; however, the video images would not be seen on screen **30**. Again as with the first embodiment, a remote video device **60** could receive video images and remotely display and record the same.

Although FIG. **8** illustrates the video processor board **50** located within the communication device **22**, the video processor board **50** may alternatively be co-located with the imaging device **40** within the distal tip of the camera module **10'**. Accordingly, all necessary video processing may take place within the camera module and the video signal which would be transmitted by the radio transceiver element **88** is a post video signal which is ready for viewing by either the video monitor **30**, or the remote video device **60** once the transceiver radio module **84** receives, authenticates, and strips the video signal of its carrier frequency as transmitted by the radio transceiver element **88**.

FIG. **9** is a schematic diagram illustrating one way in which the imaging device **11** may be constructed. As illustrated, the image sensor **40** may include the timing and control circuits on the same planar structure. Power is supplied to image sensor **40** by power supply board **64**. The connection between image sensor **40** and board **64** may simply be a cable having two conductors therein, one for ground and another for transmitting the desired voltage. These are illustrated as conductors **44** and **46**. The output from image sensor **40** in the form of the pre-video signal is input to video processor board **50** by means of the conductor **48**. In the configuration of FIG. **4**, conductor **48** may simply be a 50 ohm conductor. Power and ground also are supplied to video processing board **50** by conductors **44** and **46** from power supply board **52**. The output signal from the video processor board **50** is in the form of the post-video signal and which may be carried by conductor **49** which can also be a 50 ohm conductor. As discussed above with respect to the second embodiment, in lieu of a hard wired connection by use of conductors **48** and **49**, the pre-video signal or the post-video signal (depending upon the configuration of the imaging device) is transmitted wirelessly to the transceiver radio module **84**.

Although FIG. **9** illustrates the image sensor and the timing and control circuits being placed on the same circuit board or planar structure, it is possible to separate the timing and control circuits from the pixel array and place the timing and control circuits onto video processing board **50**. The advantage in placing the timing and control circuits on the same planar structure as the image sensor is that only three connections are required between image sensor **40** and the rest of the imaging device, namely, conductors **44**, **46** and **48**. Additionally, placing the timing and control circuits on the same planar structure with the pixel array results in the pre-video signal having less noise. Furthermore, the addition of the timing and control circuits to the same planar structure carrying the image sensor only adds a negligible amount of size to one dimension of the planar structure. If the pixel array is to be the only element on the planar structure, then additional connections must be made between the planar structure and the video processing board **50** in order to transmit the clock signals and other control signals to the pixel array. For example, a ribbon-type cable (not shown) or a plurality of 50 ohm coaxial cables (not shown) must be used in order to control the downloading of information from the pixel array. Each of these additional connections would be hard wired between the boards.

FIG. **9***a* is a more detailed schematic diagram of image sensor **40** which contains an array of pixels **90** and the timing and control circuits **92**. One example of a pixel array **90** which can be used within the invention is similar to that which is disclosed in U.S. Pat. No. 5,471,515 to Fossum, et al., said patent being incorporated by reference herein. More specifically, FIG. **3** of Fossum, et al. illustrates the circuitry which makes up each pixel in the array of pixels **90**. The array of pixels **90** as described in Fossum, et al. is an active pixel group with intra-pixel charged transfer. The image sensor made by the array of pixels is formed as a monolithic complementary metal oxide semiconductor (CMOS) integrated circuit which may be manufactured in an industry standard complementary metal oxide semiconductor process. The integrated circuit includes a focal plane array of pixel cells, each one of the cells including a photo gate overlying the substrate for accumulating the photo generated charges. In broader terms, as well understood by those skilled in the art, an image impinges upon the array of pixels, the image being in the form of photons which strike the photo diodes in the array of pixels. The photo diodes or photo detectors convert the photons into electrical energy or electrons which are stored in capacitors found in each pixel circuit. Each pixel circuit has its own amplifier which is controlled by the timing and control circuitry discussed below. The information or electrons stored in the capacitors is unloaded in the desired sequence and at a desired frequency, and then sent to the video processing board **50** for further processing.

Although the active pixel array disclosed in U.S. Pat. No. 5,471,515 is mentioned herein, it will be understood that the hybrid CCD/CMOS described above, or any other solid state imaging device may be used wherein timing and control circuits can be placed either on the same circuit board or planar structure with the pixel array, or may be separated and placed remotely. Furthermore, it will be clearly understood that the invention claimed herein is not specifically limited to an image sensor as disclosed in the U.S. Pat. No. 5,471,515, but encompasses any image sensor which may be configured for use in conjunction with the other processing circuitry which makes up the imaging device of this invention.

To summarize the different options available in terms of arrangement of the components of the imaging device **11**, the array of pixels **90** of the image sensor **40** may be placed alone on a first plane, or the timing and control circuitry **92** may be placed with the array of pixels **90** on the first plane. If the timing and control circuitry **92** is not placed with the array of pixels **90** on the first plane, the timing and control circuitry **92** may be placed by itself on a second plane, or the timing and control circuitry **92** may be placed on a second plane with some or all of the processing circuitry from video processing board **50**. The video processing board **50** itself may be placed on one or more planes on corresponding circuit boards containing video processing circuitry. FIG. **1***a* illustrates a single video processor board **50** located directly behind image sensor **40**; however, it shall be understood that additional circuit boards containing additional circuitry may be placed behind the image sensor **40** and behind the video processing board **50**. Some or all of the video processing circuitry may be placed within the camera module **10** near the distal end thereof adjacent the image sensor **40**. Video processing circuitry which is not placed within the distal end of the camera module **10** may be placed within the housing **24** of the communication device. If video processing cir-

cuitry is placed near the distal end of the camera module **10**, it is preferable to arrange the video processing circuitry in a stacked relationship behind the image sensor **40**. Additionally, it is preferable to place the processing circuitry in a parallel arrangement with respect to image sensor **40** and to center such video processing circuitry along axis X—X in order to minimize the size of camera module **10**.

The timing and control circuits **92** are used to control the release of the image information or image signal stored in the pixel array. In the image sensor of Fossum, et al., the pixels are arranged in a plurality of rows and columns. The image information from each of the pixels is first consolidated in a row by row fashion, and is then downloaded from one or more columns which contain the consolidated information from the rows. As shown in FIG. **9***a*, the control of information consolidated from the rows is achieved by latches **94**, counter **96**, and decoder **98**. The operation of the latches, counter and decoder is similar to the operation of similar control circuitry found in other imaging devices. That is, a latch is a means of controlling the flow of electrons from each individual addressed pixel in the array of pixels. When a latch **94** is enabled, it will allow the transfer of electrons to the decoder **98**. The counter **96** is programmed to count a discrete amount of information based upon a clock input from the timing and control circuits **92**. When the counter **96** has reached its set point or overflows, the image information is allowed to pass through the latches **94** and be sent to the decoder **98** which places the consolidated information in a serial format. Once the decoder **98** has decoded the information and placed it in the serial format, then the row driver **100** accounts for the serial information from each row and enables each row to be downloaded by the column or columns. In short, the latches **94** will initially allow the information stored in each pixel to be accessed. The counter **96** then controls the amount of information flow based upon a desired time sequence. Once the counter has reached its set point, the decoder **98** then knows to take the information and place it in the serial format. The whole process is repeated, based upon the timing sequence that is programmed. When the row driver **100** has accounted for each of the rows, the row driver reads out each of the rows at the desired video rate.

The information released from the column or columns is also controlled by a series of latches **102**, a counter **104** and a decoder **106**. As with the information from the rows, the column information is also placed in a serial format which may then be sent to the video processing board **50**. This serial format of column information is the pre-video signal carried by conductor **48**. The column signal conditioner **108** places the column serial information in a manageable format in the form of desired voltage levels. In other words, the column signal conditioner **108** only accepts desired voltages from the downloaded column(s).

The clock input to the timing and control circuits **92** may simply be a quartz crystal timer. This clock input is divided into many other frequencies for use by the various counters. The run input to the timing and control circuit **92** may simply be an on/off control. The default input can allow one to input the pre-video signal to a video processor board which may run at a frequency of other than 30 hertz. The data input controls functions such as zoom. At least for a CMOS type active pixel array which can be accessed in a random manner, features such as zoom are easily manipulated by addressing only those pixels which locate a desired area of interest by the user.

A further discussion of the timing and control circuitry which may be used in conjunction with an active pixel array is disclosed in U.S. Pat. No. 5,471,515 and is also described in an article entitled "Active Pixel Image Sensor Integrated With Readout Circuits" appearing in *NASA Tech Briefs*, October 1996, pp. 38 and 39. This particular article is also incorporated by reference.

Once image sensor **40** has created the pre-video signal, it is sent to the video processing board **50** for further processing. At board **50**, as shown in FIG. **9***b*, the pre-video signal is passed through a series of filters. One common filter arrangement may include two low pass filters **114** and **116**, and a band pass filter **112**. The band pass filter only passes low frequency components of the signal. Once these low frequency components pass, they are then sent to detector **120** and white balance circuit **124**, the white balance circuit distinguishing between the colors of red and blue. The white balance circuit helps the imaging device set its normal, which is white. The portion of the signal passing through low pass filter **114** then travels through gain control **118** which reduces the magnitude or amplitude of this portion to a manageable level. The output from gain control **118** is then fed back to the white balance circuit **124**. The portion of the signal traveling through filter **116** is placed through the processor **122**. In the processor **122**, the portion of the signal carrying the luminance or non-chroma is separated and sent to the Y chroma mixer **132**. Any chroma portion of the signal is held in processor **122**.

Referring to the output of the white balance circuit **124**, this chroma portion of the signal is sent to a delay line **126** where the signal is then further reduced by switch **128**. The output of switch **128** is sent through a balanced modulator **130** and also to the Y chroma mixer **132** where the processed chroma portion of the signal is mixed with the processed non-chroma portion. Finally, the output from the Y chroma mixer **132** is sent to the NTSC/PAL encoder **134**, commonly known in the art as a "composite" encoder. The composite frequencies are added to the signal leaving the Y chroma mixer **132** in encoder **134** to produce the post-video signal which may be accepted by a television. Additionally, the signal from Y chroma mixer **132** is sent to the digital signal processor **72** so that images can be viewed on monitor **30**.

In addition to the functions described above that are achieved by the digital signal processor **72**, the processor **72** can also provide additional digital enhancements. Specifically, digital enhancement can sharpen or otherwise clarify the edges of an image viewed on a video screen which might normally be somewhat distorted. Additionally, selected background or foreground images may be removed thus only leaving the desired group of images.

In addition to digital enhancement, the digital signal processor **72** can include other circuitry which may further condition the signal received from board **50** so that it may be viewed in a desired format other than NTSC/PAL. One common encoder which can be used would be an RGB encoder. An RGB encoder separates the signal into the three primary colors (red, green and blue). A SVHS encoder (super video home system) encoder could also be added to processor **72**. This type of encoder splits or separates the luminance portion of the signal and the chroma portion of the signal. Some observers believe that a more clear signal is input to the video device by such a separation, which in turn results in a more clear video image viewed on the video device. Another example of an encoder which could be added to processor **72** includes a VGA compatible encoder, which enables the video signal to be viewed on a standard VGA monitor which is common to many computer monitors.

One difference between the arrangement of image sensor **40** and the outputs found in FIG. **3** of the Fossum, et al. patent is that in lieu of providing two analog outputs [namely, VS out (signal) and VR out (reset)], the reset function takes place in the timing and control circuitry **92**. Accordingly, the pre-video signal only requires one conductor **48**.

FIGS. **10** *a*–**10***e* illustrate in more detail one example of circuitry which may be used in the video processing board **50** in order to produce a post-video signal which may be directly accepted by a NTSC/PAL compatible video device such as a television. The circuitry disclosed in FIGS. **10***a*–**10***e* is very similar to circuitry which is found in a miniature quarter-inch Panasonic camera, Model KS-162. It will be understood by those skilled in the art that the particular arrangement of elements found in FIGS. **10***a*–**10***e* are only exemplary of the type of video processing circuitry which may be incorporated in order to take the pre-video signal and condition it to be received by a desired video device.

As shown in FIG. **10***a*, 5 volt power is provided along with a ground by conductors **44** and **46** to board **50**. The pre-video signal carried by conductor **48** is buffered at buffer **137** and then is transferred to amplifying group **138**. Amplifying group **138** amplifies the signal to a usable level as well as achieving impedance matching for the remaining circuitry.

The next major element is the automatic gain control **140** shown in FIG. **10***b*. Automatic gain control **140** automatically controls the signal from amplifying group **138** to an acceptable level and also adds other characteristics to the signal as discussed below. More specifically, automatic gain control **140** conditions the signal based upon inputs from a 12 channel digital to analog converter **141**. Converter **141** retrieves stored information from EEPROM (electrically erasable programmable read only memory) **143**. EEPROM **143** is a non-volatile memory element which may store user information, for example, settings for color, tint, balance and the like. Thus, automatic gain control **140** changes the texture or visual characteristics based upon user inputs. The keypad **26**, in addition to the conventional buttons used to control telephone communications, could also include buttons for controlling the image viewed on monitor **30** such as a gain control **140**. The signal leaving the automatic gain control **140** is an analog signal until being converted by analog to digital converter **142**.

Digital signal processor **144** of FIG. **10***c* further processes the converted signal into a serial type digital signal. One function of the microprocessor **146** is to control the manner in which digital signal processor **144** sorts the digital signals emanating from converter **142**. Microprocessor **146** also controls analog to digital converter **142** in terms of when it is activated, when it accepts data, when to release data, and the rate at which data should be released. Microprocessor **146** may also control other functions of the imaging device such as white balance. The microprocessor **146** may selectively receive the information stored in the EEPROM **143** and carry out its various commands to further control the other elements within the circuitry.

After the signal is processed by digital signal processor **144**, the signal is sent to digital encoder **148** illustrated in FIG. **10***d*. Some of the more important functions of digital encoder **148** are to encode the digital signal with synchronization, modulated chroma, blanking, horizontal drive, and the other components necessary so that the signal may be placed in a condition for reception by a video device such as a television monitor. As also illustrated in FIG. **10***d*, once the signal has passed through digital encoder **148**, the signal is reconverted into an analog signal through digital to analog converter **150**.

This reconverted analog signal is then buffered at buffers **151** and then sent to amplifier group **152** of FIG. **10***e* which amplifies the signal so that it is readily accepted by a desired video device. Specifically, as shown in FIG. **10***e*, one SVHS outlet is provided at **160**, and two composite or NTSC outlets are provided at **162** and **164**, respectively.

From the foregoing, it is apparent that an entire imaging device may be incorporated within the distal tip of the camera module, or may have some elements of the imaging device being placed in the housing of the communication device. Based upon the type of image sensor used, the profile area of the imaging device may be made small enough to be placed into a camera module which has a very small diameter.

This invention has been described in detail with reference to particular embodiments thereof, but it will be understood that various other modifications can be effected within the spirit and scope of this invention.

What is claimed is:

1. In a wireless telephone for conducting wireless telephonic communications, the improvement comprising:

a video system integral with said telephone for receiving and transmitting video images, and for viewing said video images, said video system comprising;

a camera module housing an image sensor therein, said image sensor including an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal, a first circuit board mounted in said camera module adjacent said image sensor and electrically coupled to said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format, said camera module further including a transceiver radio element mounted therein and electrically communicating with said first circuit board to transmit said converted pre-video signal;

a transceiver radio module mounted in the wireless telephone for wirelessly communicating with said transceiver element in said camera module to receive said converted pre-video signal;

a video monitor attached to said wireless phone for viewing said video images, said video monitor electrically coupled to said transceiver radio module for displaying video images processed by said first circuit board.

2. A device, as claimed in claim **1**, wherein:

said pixels are CMOS pixels.

3. A device, as claimed in claim **1**, wherein:

said transceiver radio element and said transceiver radio module communicate by a Bluetooth communications standard.

4. A device, as claimed in claim **1**, wherein:

said transceiver radio element and said transceiver radio module communicate by an IEEE 802.15.3 communications standard.

5. In a wireless telephone for conducting wireless telephonic communications, the improvement comprising:

a video system integral with said telephone for receiving and transmitting video images, and for viewing said video images, said video system comprising;

a camera module housing an image sensor therein, said image sensor including an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal;

said camera module further including a transceiver radio element mounted therein and electrically communicating with said image sensor to transmit said pre-video signal;

a transceiver radio module mounted in the wireless telephone for wirelessly communicating with said radio transceiver element in said camera module to receive said pre-video signal;

a first circuit board mounted in said wireless telephone and electrically coupled to said transceiver radio module, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;

a video monitor attached to said wireless phone for viewing said video images, said video monitor electrically coupled to said transceiver radio module for displaying video images processed by said first circuit board.

6. A device, as claimed in claim **5**, wherein:

said pixels are CMOS pixels.

7. A device, as claimed in claim **5**, wherein:

said transceiver radio element and said transceiver radio module communicate by a Bluetooth standard.

8. A device, as claimed in claim **5**, wherein:

said transceiver radio element and said transceiver radio module communicate by an IEEE 802.15.3 standard.

9. In a video telephone for receiving and transmitting telephone communications to include video signals transmitted by the user of the phone, and video signals received from the party to whom a call was made, the video telephone including a housing, and a video monitor for viewing the video signals, the improvement comprising:

a camera module for taking video images, said camera module wirelessly communicating with circuitry within said video telephone enabling video signals to be transmitted from said camera module to said video telephone for viewing by said user or for further transmission to another party, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of said pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal, a first circuit board electrically connected to said image sensor and mounted within said camera module adjacent said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format, and a transceiver radio element mounted in said camera module and electrically coupled to said first circuit board for transmitting said converted pre-video signal wirelessly to the video telephone.

10. A device, as claimed in claim **9**, wherein:

said pixels are CMOS pixels.

11. A device, as claimed in claim **9**, wherein:

said transceiver radio element communicates with the video telephone by a Bluetooth communications standard.

12. A device, as claimed in claim **9**, wherein:

said transceiver radio element communicates with the video telephone by an IEEE 802.15.3 communications standard.

13. In a video telephone for receiving and transmitting telephone communications to include video signals transmitted by the user of the phone, and video signals received from the party to whom a call was made, the video telephone including a housing, and a video monitor for viewing the video signals, the improvement comprising:

a camera module for taking video images, said camera module wirelessly communicating with circuitry within said video telephone enabling video signals to be transmitted from said camera module to said video telephone for viewing by said user or for further transmission to another party, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of said pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal, and a transceiver radio element mounted in said camera module and electrically coupled to said image sensor board for transmitting the pre-video signal wirelessly to the video telephone, wherein the pre-video signal is further processed in the video telephone for viewing.

14. A device, as claimed in claim **13**, wherein:

said pixels are CMOS pixels.

15. A device, as claimed in claim **13**, wherein:

said transceiver radio element communicates with the video telephone by a Bluetooth communications standard.

16. A device, as claimed in claim **13**, wherein:

said transceiver radio element communicates with the video telephone by an IEEE 802.15.3 communications standard.

17. A video telephone for conducting telephonic communications including receiving and transmitting video images between two parties of a telephone call, said video telephone comprising:

an image sensor lying in a first plane including an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal;

a first circuit board electrically communicating with said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;

a camera module housing said image sensor and said first circuit board;

a transceiver radio element mounted in said camera module and communicating with said first circuit board for wirelessly transmitting the converted pre-video signal;

a transceiver radio module communicating wirelessly with said transceiver radio element for receiving the converted pre-video signal;

a transceiver/amplifier section electrically coupled to said transceiver radio module for amplifying and further transmitting the converted pre-video signal, and for receiving and amplifying video and audio signals transmitted by the other party of the telephone call;

a digital signal processor electrically coupled to said transceiver radio module and said transceiver/amplifier section, said digital signal processor further conditioning said converted pre-video signal prior to said converted pre-video signal being manipulated by said transceiver/amplifier section, and also for conditioning video and audio signals received by said transceiver/amplifier section from the other party of the telephone call;

a microphone electrically communicating with said digital signal processor for receiving sound and converting the sound to audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video monitor attached to said video phone, said video monitor for selectively displaying the converted pre-video signals, and for selectively displaying video images received by said transceiver/amplifier section from the other party of the telephone call;

a video switch communicating with said transceiver radio module and said digital signal processor for switching video images to be viewed on said video monitor, a user being able to selectively display video images from the converted pre-video signal or video images received by the transceiver/amplifier section from the other party of the telephone call; and

a power supply mounted to said video telephone for providing power thereto.

18. A device, as claimed in claim **17**, wherein:

said pixels are CMOS pixels.

19. A device, as claimed in claim **17**, wherein:

said transceiver radio element communicates with the video telephone by a Bluetooth communications standard.

20. A device, as claimed in claim **17**, wherein:

said transceiver radio element communicates with the video telephone by an IEEE 802.15.3 communications standard.

21. A video telephone for conducting telephonic communications including receiving and transmitting video images between two parties of a telephone call, said video telephone comprising:

an image sensor lying in a first plane, and an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal;

a camera module housing said image sensor therein;

a transceiver radio element mounted in said camera module and communicating with said image sensor for wirelessly transmitting the pre-video signal;

a transceiver radio module communicating wirelessly with said transceiver radio element for receiving the pre-video signal;

a first circuit board electrically communicating with said transceiver radio module, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;

a transceiver/amplifier section electrically coupled to said first circuit board for amplifying and further transmitting the converted pre-video signal, and for receiving and amplifying video and audio signals transmitted by the other party of the telephone call;

a digital signal processor electrically coupled to said first circuit board and said transceiver/amplifier section, said digital signal processor further conditioning said converted pre-video signal prior to said converted pre-video signal being manipulated by said transceiver/amplifier section, and also for conditioning the video and audio signals received by said transceiver/amplifier section from the other party of the telephone call;

a microphone electrically communicating with said digital signal processor for receiving sound and converting the sound to audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video monitor attached to said video phone, said video monitor for selectively displaying the converted pre-video signals, and for selectively displaying video images received by said transceiver/amplifier section from the other party of the telephone call;

a video switch communicating with said transceiver radio module and said digital signal processor for switching video images to be viewed on said video monitor, a user being able to selectively display video images from the converted pre-video signal or video images received by the transceiver/amplifier section from the other party of the telephone call; and

a power supply mounted to said video telephone for providing power thereto.

22. A device, as claimed in claim **21**, wherein:

said pixels are CMOS pixels.

23. A device, as claimed in claim **21**, wherein:

said transceiver radio element communicates with the video telephone by a Bluetooth communications standard.

24. A device, as claimed in claim **21**, wherein:

said transceiver radio element communicates with the video telephone by an IEEE 802.15.3 communications standard.

25. In a wireless telephone for conducting wireless telephonic communications, the improvement comprising:

a video system integral with said telephone for receiving and transmitting video images, and for viewing said images, said video system comprising:

a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, circuitry means electrically coupled to said array of pixels for timing and control of said array of pixels, said circuitry means for timing and control being placed remote from said array of pixels on a second plane, said image sensor producing a pre-video signal, a first circuit board lying in a third plane and electrically coupled to said image sensor, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format, a transceiver radio element communicating with said first circuit board for transmitting said converted pre-video signal;

a transceiver radio module mounted in said telephone for wirelessly receiving said converted pre-video signal; and

a video monitor attached to said wireless phone for viewing said video images, said video monitor communicating with said transceiver radio module, and displaying video images processed by said first circuit board.

26. A device, as claimed in claim **25**, wherein:

said pixels are CMOS pixels.

27. A device, as claimed in claim 25, wherein:
said transceiver radio element communicates with the video telephone by a Bluetooth communications standard.

28. A device, as claimed in claim 25, wherein:
said transceiver radio element communicates with the video telephone by an IEEE 802.15.3 communications standard.

29. In a video telephone for receiving and transmitting telephone communications to include video signals transmitted by the user of the phone, and video signals received from the party to whom a call is made, the video telephone including a video monitor for viewing the video signals, the improvement comprising:
a camera module for taking video images, said camera module communicating with circuitry within said video telephone enabling video signals to be transmitted from said camera module to said video telephone for viewing by said user or for further transmission to another party, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal, a first circuit board mounted adjacent said image sensor and electrically connected to said image sensor, said first circuit board including circuitry means for timing and control of said array of pixels and circuitry means for processing and converting said pre-video signal to a desired video format, and a transceiver radio element communicating with said first circuit board for wirelessly transmitting said converted pre-video signal.

30. A device, as claimed in claim 29, wherein:
said pixels are CMOS pixels.

31. A device, as claimed in claim 29, wherein:
said transceiver radio element transmits by a Bluetooth communications standard.

32. A device, as claimed in claim 29, wherein:
said transceiver radio element transmits by an IEEE 802.15.3 communications standard.

33. In a video telephone for receiving and transmitting telephone communications to include video signals transmitted by the user of the phone, and video signals received from the party to whom a call is made, the video telephone including a video monitor for viewing the video signals, the improvement comprising:
a camera module for taking video images, said camera module communicating with circuitry within said video enabling video signals to be transmitted from said camera module to said video telephone for viewing by said user or for further transmission to another party, said camera module including an image sensor housed therein and lying in a first plane, said image sensor including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal, and a transceiver radio element communicating with said image sensor for wirelessly transmitting said pre-video signal.

34. A device, as claimed in claim 33, wherein:
said pixels are CMOS pixels.

35. A device, as claimed in claim 33, wherein:
said transceiver radio element transmits by a Bluetooth communications standard.

36. A device, as claimed in claim 33, wherein:
said transceiver radio element transmits by an IEEE 802.15.3 communications standard.

37. In a video telephone for receiving and transmitting telephone communications to include video signals transmitted by the user of the phone, and video signals received from the party to whom a call was made, the video telephone including a video monitor for viewing the video signals, the improvement comprising:
a camera module for taking video images, said camera module communicating with circuitry within said video enabling video signals to be transmitted from said camera module to said video telephone for viewing by said user or for further transmission to another party, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of said pixels for timing and control of said array of pixels, said circuitry means for timing and control placed remote from said array of pixels on a second plane, said image sensor producing a pre-video signal, a first circuit board electrically connected to said image sensor and lying in a third plane, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format, and a radio transceiver element communicating with said first circuit board for wirelessly transmitting said converted pre-video signal.

38. A device, as claimed in claim 37, wherein:
said pixels are CMOS pixels.

39. A device, as claimed in claim 37, wherein:
said transceiver radio element transmits by a Bluetooth communications standard.

40. A device, as claimed in claim 37, wherein:
said transceiver radio element transmits by an IEEE 802.15.3 communications standard.

41. In a video telephone for receiving and transmitting telephone communications to include video signals transmitted by the user of the phone, and video signals received from the party to whom a call was made, the video telephone including a video monitor for viewing the video signals, the improvement comprising:
a camera module for taking video images, said camera module communicating with circuitry within said video telephone enabling viewing of said video images on said video telephone and enabling video signals to be transmitted from said camera module for viewing by said party, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of said pixels for timing and control of said array of pixels, said circuitry means for timing and control placed remote from said array of pixels on a second plane, said image sensor producing a pre-video signal, and a radio transceiver element communicating with said image sensor for wirelessly transmitting said pre-video signal.

42. A device, as claimed in claim 41, wherein:
said pixels are CMOS pixels.

43. A device, as claimed in claim 41, wherein:
said transceiver radio element transmits by a Bluetooth communications standard.

44. A device, as claimed in claim 41, wherein:
said transceiver radio element transmits by an IEEE 802.15.3 communications standard.

45. A video telephone for conducting telephonic communications including receiving and transmitting video images between two parties of a telephone call, said video telephone comprising:

an image sensor lying in a first plane including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal;

a first circuit board electrically communicating with said image sensor, said first circuit board including circuitry means for timing and control of said array of pixels and circuitry means for processing and converting said pre-video signal to a desired video format;

a transceiver radio element communicating with said first circuit board for wirelessly transmitting said converted pre-video signal;

a camera module housing said image sensor, said first circuit board, and said transceiver radio element therein;

a transceiver radio module mounted in said telephone for receiving said converted pre-video signal;

a transceiver/amplifier section electrically coupled to said transceiver radio module for amplifying and further transmitting the converted pre-video signal, and for receiving and amplifying video and audio signals transmitted by the other party of the telephone call;

a digital signal processor electrically coupled to said transceiver radio module and said transceiver/amplifier section, said digital signal processor further conditioning said pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals received by said transceiver/amplifier section from the other party of the telephone call;

a microphone electrically communicating with said digital signal processor for receiving sound and converting the sound to audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video monitor attached to said video phone, said video monitor for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section;

a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video monitor; and

a power supply mounted to said video telephone for providing power thereto.

46. A device, as claimed in claim **45**, wherein:

said pixels are CMOS pixels.

47. A device, as claimed in claim **45**, wherein:

said transceiver radio element transmits by a Bluetooth communications standard.

48. A device, as claimed in claim **45**, wherein:

said transceiver radio element transmits by an IEEE 802.15.3 communications standard.

49. A video telephone for conducting telephonic communications including receiving and transmitting video images between two parties of a telephone call, said video telephone comprising:

an image sensor lying in a first plane including an array of pixels for receiving images thereon, said image sensor producing a pre-video signal;

a first circuit board electrically communicating with said image sensor, said first circuit board including circuitry means for timing and control of said array of pixels;

a transceiver radio element communicating with said first circuit board for wirelessly transmitting said pre-video signal;

a camera module housing said image sensor, said first circuit board, and said transceiver radio element therein;

a transceiver radio module mounted in said telephone for receiving said pre-video signal;

a second circuit board electronically communicating with said radio transceiver module, said second circuit board including circuitry means for converting said pre-video signal to a desired video format;

a transceiver/amplifier section electrically coupled to said second circuit board for amplifying and further transmitting said converted pre-video signal, and for receiving and amplifying video and audio signals transmitted by the other party of the telephone call;

a digital signal processor electrically coupled to said second circuit board and said transceiver/amplifier section, said digital signal processor further conditioning said converted pre-video signal which is first conditioned by said second circuit board, and also for conditioning video and audio signals received by said transceiver/amplifier section from the other party of the telephone call;

a microphone electrically communicating with said digital signal processor for receiving sound and converting the sound to audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video monitor attached to said video phone, said video monitor for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section from the other party of the telephone call;

a video switch communicating with said second circuit board and said digital signal processor for switching video images to be viewed on said video monitor, a user being able to selectively display video images from the imaging device or video images received by the transceiver/amplifier section from the other party of the telephone call; and

a power supply mounted to said video telephone for providing power thereto.

50. A device, as claimed in claim **49**, wherein:

said pixels are CMOS pixels.

51. A device, as claimed in claim **49**, wherein:

said transceiver radio element transmits by a Bluetooth communications standard.

52. A device, as claimed in claim **49**, wherein:

said transceiver radio element transmits by an IEEE 802.15.3 communications standard.

53. A video telephone for conducting telephonic communications including receiving and transmitting video images between two parties of a telephone call, said video telephone comprising:

an image sensor lying in a first plane, and an array of pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of pixels for timing and control of said array of pixels, said circuitry means for timing and control being placed remote from said array of pixels on a second plane, said image sensor producing a pre-video signal;

a first circuit board electrically coupled with said image sensor and lying in a third plane, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format;

a transceiver radio element communicating with said first circuit board to wirelessly transmit the converted pre-video signal;

a camera module housing said image sensor, said first circuit board and said transceiver radio element;

a transceiver radio module mounted in said videophone for wirelessly receiving said converted pre-video signal,

a transceiver/amplifier section electrically coupled to said transceiver radio module for amplifying and further transmitting said converted pre-video signal and for receiving and amplifying video and audio signals transmitted by the other party of the telephone call;

a digital signal processor electrically coupled to said transceiver radio module and said transceiver/amplifier section, said digital signal processor further conditioning said converted pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals received by said transceiver/amplifier section from the other party of the telephone call;

a microphone electrically communicating with said digital signal processor for receiving sound and converting the sound to audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

a video monitor attached to said video phone, said video monitor for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section from the other party of the telephone call;

a video switch communicating with said transceiver radio module and said digital signal processor for switching video images to be viewed on said video monitor, a user being able to selectively display video images from the imaging device or video images received by the transceiver/amplifier section from the other party of the telephone call; and

a power supply mounted to said video telephone for providing power thereto.

54. A device, as claimed in claim **53**, wherein:

said pixels are CMOS pixels.

55. A device, as claimed in claim **53**, wherein:

said transceiver radio element transmits by a Bluetooth communications standard.

56. A device, as claimed in claim **53**, wherein:

said transceiver radio element transmits by an IEEE 802.15.3 communications standard.

57. In a method for conducting video telephone communications with a video telephone, the improvement comprising the steps of:

providing a camera module having an image sensor housed therein;

removing the camera module from connection with the video telephone;

pointing the camera module at a targeted object and selectively taking video images of the targeted object;

wirelessly transmitting the video images taken by the image sensor to the video telephone;

processing the video images transmitted by the camera module; and

selectively viewing the video images on the video telephone and selectively transmitting the video images to another party.

58. A method, as claimed in claim **57**, wherein:

said image sensor includes a CMOS pixel array.

59. In a wireless telephone for conducting wireless telephonic communications, the improvement comprising:

a camera module housing an image sensor therein, said camera module for producing video images of a targeted object;

means for wirelessly interconnecting said camera module to said wireless telephone, said means for wirelessly interconnecting enabling said camera module to be selectively displaced away from and not in contact with said wireless telephone; and

a video monitor attached to said wireless phone for selectively viewing video images taken by said camera module, and for selectively viewing incoming video images transmitted by another party.

60. A device, as claimed in claim **59**, wherein:

said video telephone includes a housing, and an opening in said housing for receiving said camera module so as to place said camera module in a stored position.

61. In a video telephone for conducting communications including receiving and transmitting video images between two parties of a video telephone call, the improvement comprising:

a camera module housing an image sensor therein;

a camera module battery housed within said camera module for providing power to said camera module;

a camera battery charge circuit housed within the video telephone;

a telephone battery housed within the telephone for providing power to said camera battery charge circuit; and

wherein the camera module is received in the video telephone so said camera module battery electrically communicates with said camera battery charge circuit to selectively charge said camera module battery.

62. A method of powering and recharging a camera module for use with a video telephone, said method comprising the steps of:

providing a video telephone including a camera battery charge circuit and a telephone battery housed therein;

providing a camera module housing an image sensor therein for taking video images, and a camera module battery housed within said camera module for selectively powering said camera module;

removing said camera module from seated engagement with the video telephone resulting in activation of said camera module battery for powering said camera module; and

returning said camera module to its seated position with said video telephone and in electrical communication with the battery charge circuit to charge said camera module battery.

* * * * *

CERTIFICATE OF COMPLIANCE WITH FED. CIR. R. 32

1. The foregoing filing complies with the type-volume limitation of Fed. Cir. R. 32(b)(1) because this brief contains 12,052 words exclusive of the parts of the filing as exempted by Fed. Cir. R. 32(b)(2).

2. This brief complies with the typeface requirements of Fed. R. App. P. 32(a)(5) and the type style requirements of Fed. R. App. P. 32(a)(6) because this brief has been prepared in a proportionally spaced typeface using Microsoft Word 2016 in Times New Roman 14 point font.

Dated: May 16, 2022

/s/ Paul J. Andre
Paul J. Andre